



H81H3-AM

Rev:1.0

TABLE OF CONTENTS

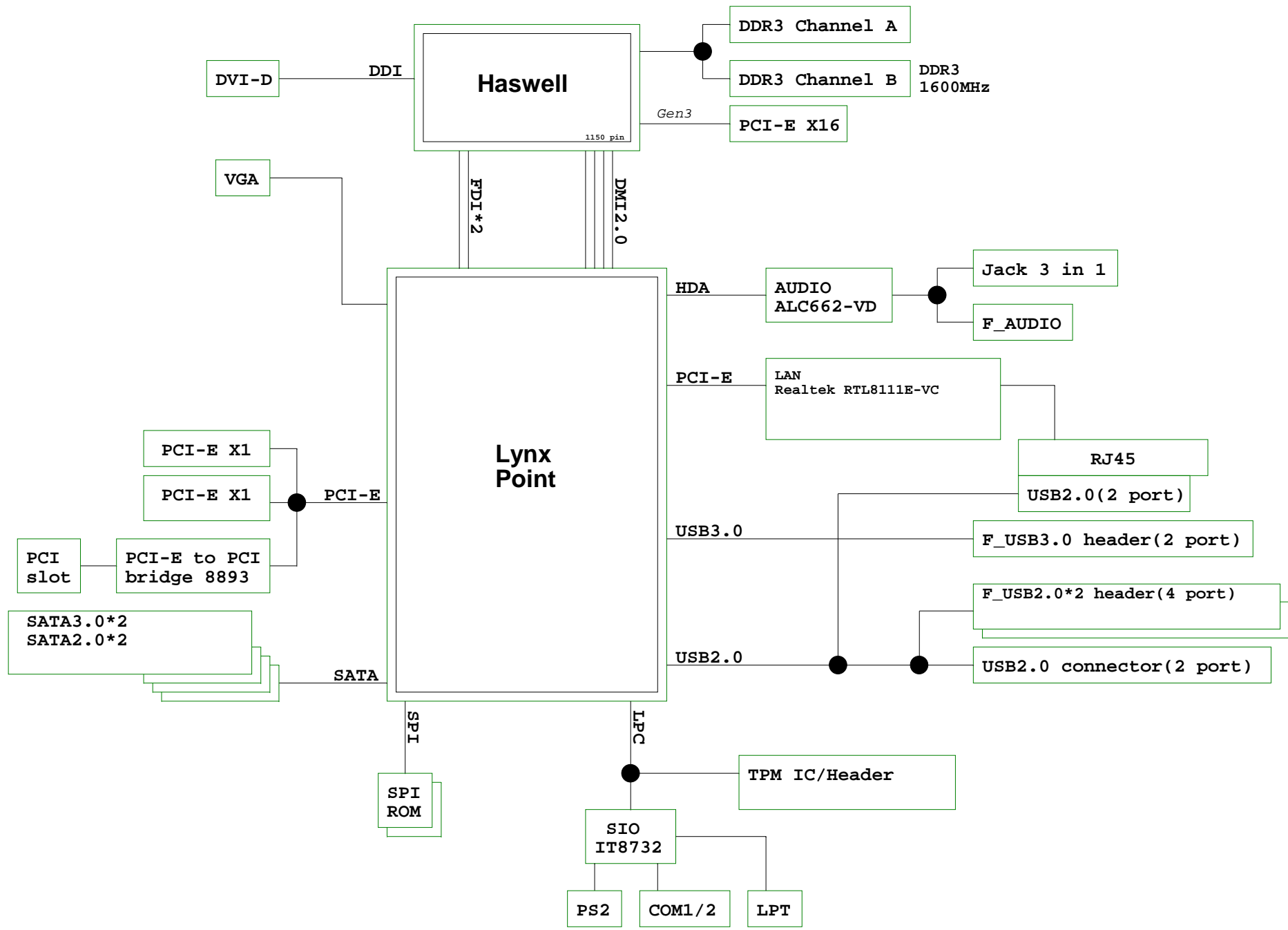
Page	Index
1	Cover Page
2	Block Diagram
3	GPIO Function & INT# Mapping
4	CPU-PEG/DMI/FDI/DDI
5	CPU-MISC
6	CPU-DDR3
7	CPU-POWER
8	CPU-GND
9	PCIE*16
10	DVI-D+VGA
11	DDR3-CHA/CHB
12	DDR3-Vref
13	PCH-DMI/PE/USB2.0
14	PCH-FDI/DDI/USB3.0/CLK
15	PCH-SATA/SATA CONN & PWR/OBR
16	PCH-MISC
17	PCH-POWER
18	PCH-GND
19	PCIE*1
20	PCI Bridge-IT8893
21	PCI Slot
22	USB2.0 CONN & Header
23	USB3.0 Header
24	SPI/SMbus
25	ECIO-IT8732
26	FAN/PS2/Buzzer/F_Panel

Page	Index
27	LPT/COM/TPM
28	LAN RTL8111E-VC
29	AUDIO-ALC662_VD
30	AUDIO-CONN & Header
31	XDP-CPU/PCH
32	DC/DC VDIMM/DDR_VTT/5VDUAL
33	DC/DC PCH_1.5V/PCH_ME_1.05V
34	DC/DC ATX_3VSB/3VDUAL
35	DC/DC Vcore /Gate driver
36	DC/DC VCC3 & VCC & ATX12P
37	PWR Delivery
38	PWR Sequence/RST Diagram
39	CLK Distribution

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REVISION HISTORY:

Rev	Date	Notes
A		



PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO13	3VSB	LPC_PME	GPI
GPIO40	3VSB	USB_5VDUAL control (reserve)	Native
GPIO72	3VSB	USB_5VDUAL control	Native
GPIO45	3VSB	BIOS WP	Native
GPIO57	3VSB	BIOS WP	GPI
GPIO46	3VSB	WLAN_DIS_L	Native
GPIO61	3VSB	LPCPD_L	Native
GPIO27	ATX_3VSB	ILAN_WAKE_L	GPI
GPIO1	VCC3	OBR	GPI
GPIO6	VCC3	Thermal_SD	GPI
GPIO68	VCC3	TP_VGA	GPI
GPIO23	VCC3	HDPANEL_DETECT	Native
GPIO15	3VSB	PEX16_RST	GPO
DL,BIOS must be pro			
GPIO73	3VSB	case open(reserve)	PCIECLKRQ0#
GPIO24	3VSB	ME_Disable	GPO
GPIO19	VCC3	BOOT device detect	GPI
GPIO51	VCC3	BOOT device detect	GPO

Interrupt mapping

Function	INT# port	PCle*1 port	Device
PCI Bridge	INTB#	port 2	IC IT8893
LAN	INTC#	port 3	RTL8111E-VC
PCIEX1	INTD#	port 4	LPT integrate
PCIEX1	INTA#	port 5	LPT integrate
SATA	INTB#	NA	LPT integrate

SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16	VCC3	Beep(reserve)	CIRRX2
GP31	3VSB	Thermal_SD	PWMOUT
GP35	3VSB	LED0	FAN_TAC4
GP37	3VSB	LED1	FAN_TAC3
GP70	VCC3	TPM Onboard detect	GPIO
GP71	VCC3	BOM detect	GPIO
GP73	VCC3	BOM detect	GPIO
GP74	VCC3	BOM detect	GPIO
GP75	VCC3	BOM detect	GPIO
GP76	VCC3	Thermal_HD_Auto_Switch	GPIO
GP46	3VSB	Acer Header	GPIO
GP47	3VSB	Acer Header	GPIO
GP40	3VSB	5VDUAL Switch	3VSB5W
RI1#	3VSB	LAN on MB wake up	RI1

BIOS must be pro to Native 3VSB5W

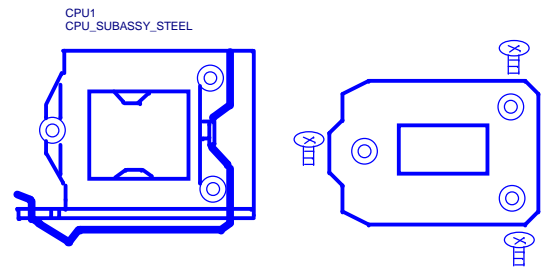


2012/09/20
 remove R for PDG1.0

14 FDI_CSYSN >> FDI_CSYSN D16
 14 FDI_INT >> FDI_INT D18
 14 CK_DP_SSC_N >> CK_DP_SSC_N U5
 14 CK_DP_SSC_P >> CK_DP_SSC_P U6

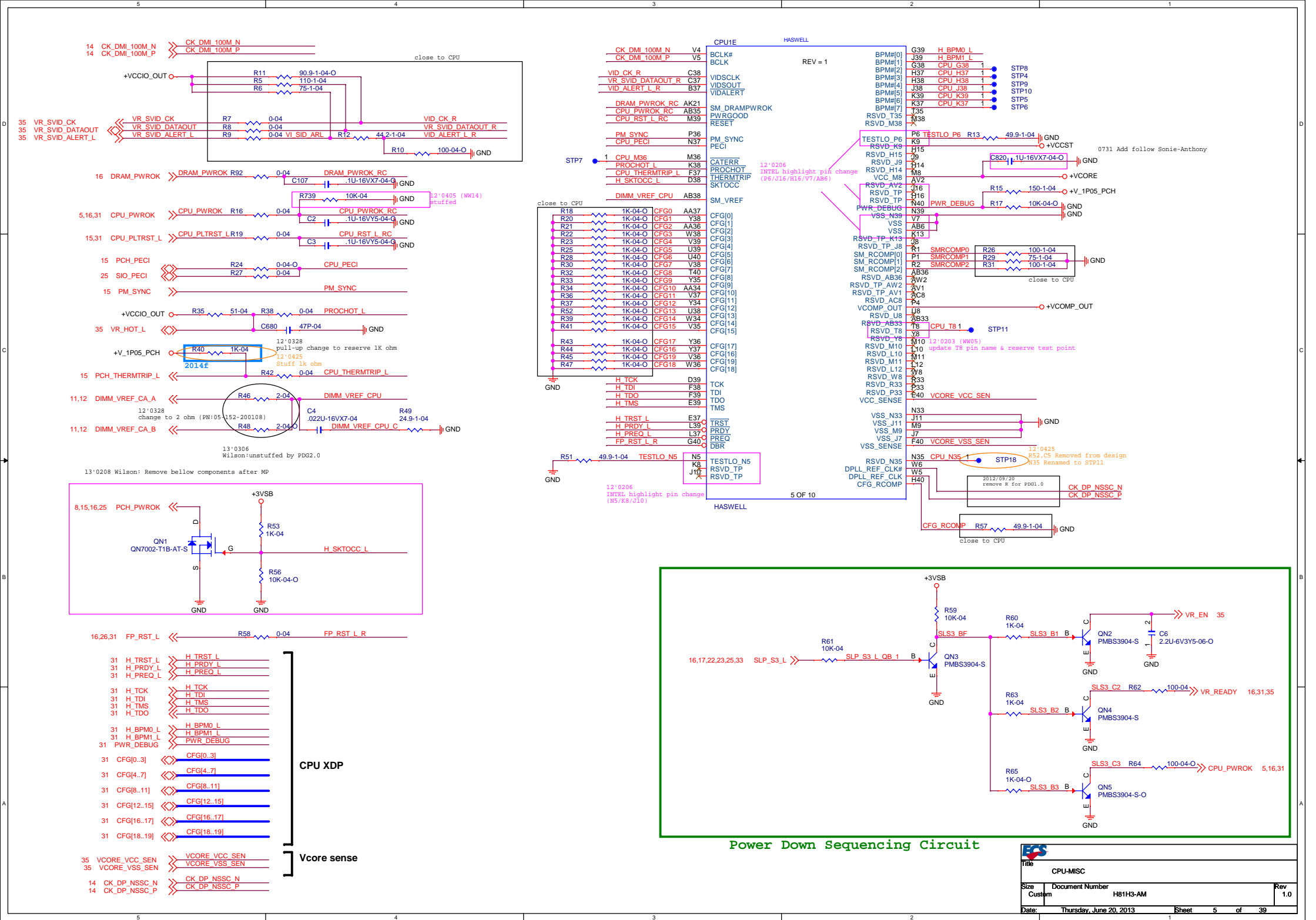
STP1 1 CPU E16 E16
 STP2 1 CPU K11 K11
 STP3 1 CPU J12 J12

14 FDI_TX_N0 >> FDI_TX_N0 B14
 14 FDI_TX_P0 >> FDI_TX_P0 A14
 14 FDI_TX_N1 >> FDI_TX_N1 C13
 14 FDI_TX_P1 >> FDI_TX_P1 B13



CPU steel (T/U pahse)
 PN:20-800-005711 CPU SOCKET STEEL SUBASSY.STEEL...LGA 1155/1156P.W/BACK PLATE,CAP.LOTES

CPU socket (SMD phase)
 PN:11-018-115128 SOCKET.CPU..LGA 1150P SMD..15u...BLACK.ACA-ZIF-138-P01...HF.LEAD-FREE.LOTES



11	M_DATA_A[0..63]	<<	M_DATA A[0..63]
11	M_DQS_A_P[0..7]	<<	M_DQS A P[0..7]
11	M_DQS_A_N[0..7]	<<	M_DQS A N[0..7]
11	M_MA_A[0..15]	<<	M_MA A[0..15]
11	M_BS_A[0..2]	<<	M_BS A[0..2]
11	M_CS_A_L[0..1]	<<	M_CS A L[0..1]
11	M_CKE_A[0..1]	<<	M_CKE A[0..1]
11	M_ODT_A[0..1]	<<	M_ODT A[0..1]
11	M_CLK_A_P[0..1]	<<	M_CLK A P[0..1]
11	M_CLK_A_N[0..1]	<<	M_CLK A N[0..1]
11	M_WE_A_L	<<	M_WE A_L
11	M_CAS_A_L	<<	M_CAS A_L
11	M_RAS_A_L	<<	M_RAS A_L

DDR3 CH.A

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11	M_MA_B[0..15]	<<	M_MA B[0..15]
11	M_BS_B[0..2]	<<	M_BS B[0..2]
11	M_CS_B_L[0..1]	<<	M_CS B L[0..1]
11	M_CKE_B[0..1]	<<	M_CKE B[0..1]
11	M_ODT_B[0..1]	<<	M_ODT B[0..1]
11	M_CLK_B_P[0..1]	<<	M_CLK B P[0..1]
11	M_CLK_B_N[0..1]	<<	M_CLK B N[0..1]
11	M_WE_B_L	<<	M_WE B_L
11	M_CAS_B_L	<<	M_CAS B_L
11	M_RAS_B_L	<<	M_RAS B_L

DDR3 CH.B

6.11 DDR3_DRAMRST_L << DDR3_DRAMRST_L

**Attention

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M_DATA A11	AK39	SA_DQ[11]
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CPU1A

HASWELL

REV = 1

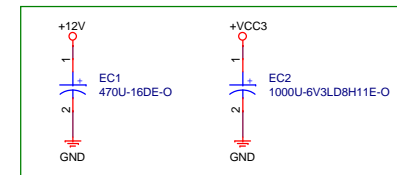
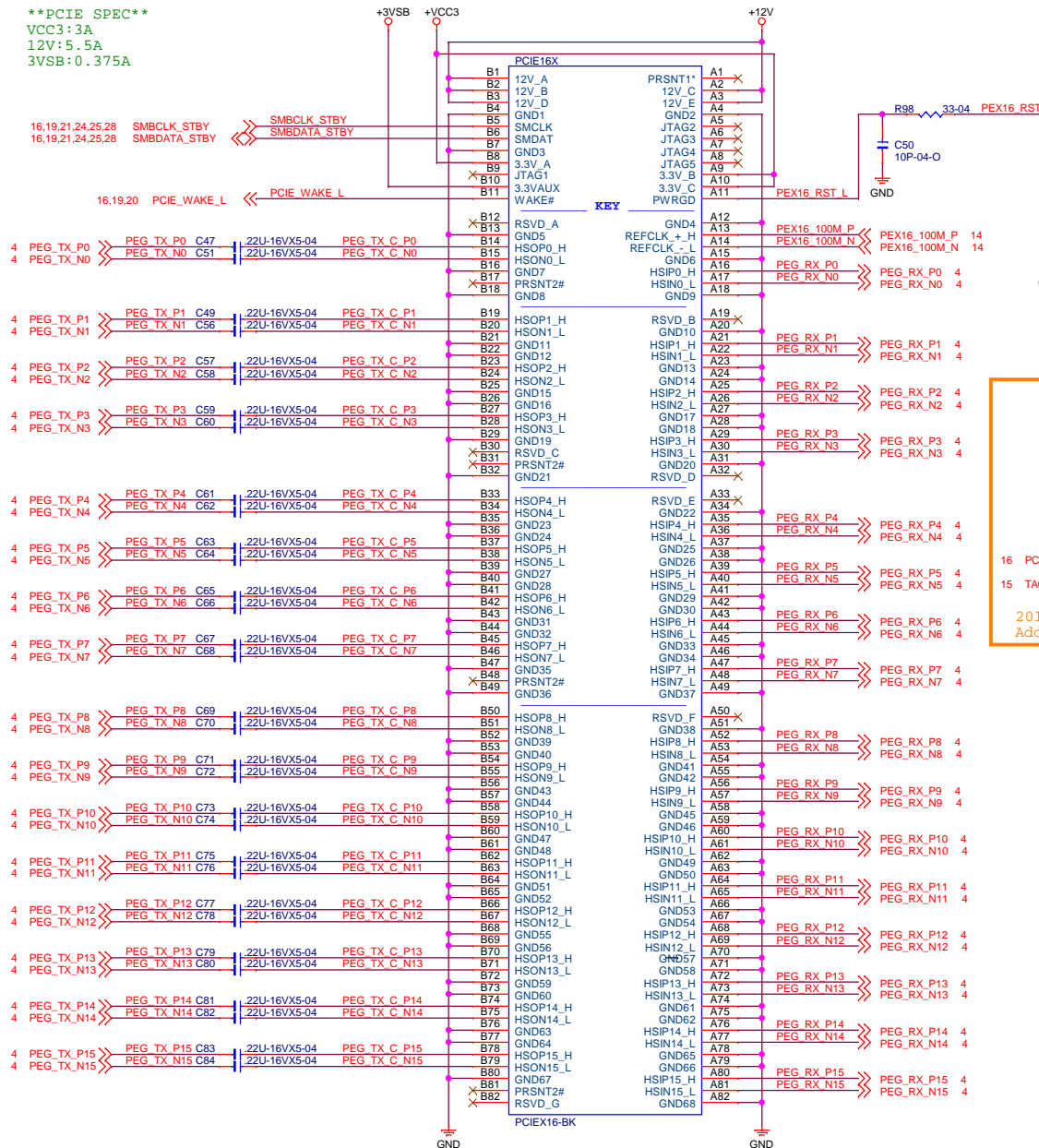
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SA_CK[95]	AW13
SA_CK[96]	AW13
SA_CK[97]	AW13
SA_CK[98]	AW13
SA_CK[99]	AW13

**Attention

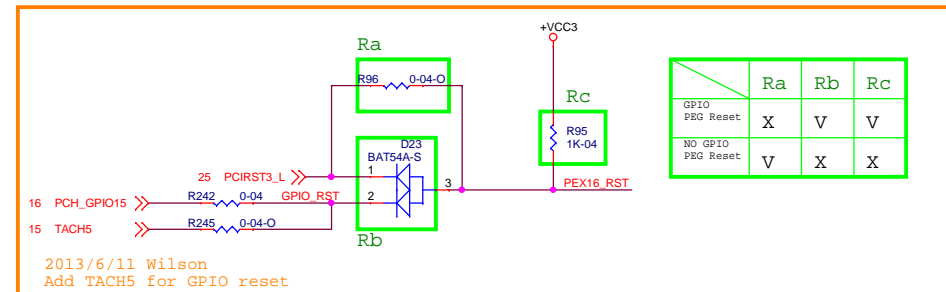
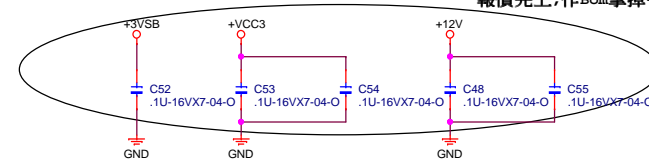
M_DATA B0	AE34	SB_DQ[0]
M_DATA B1	AE35	SB_DQ[1]
M_DATA B2	AG35	SB_DQ[2]

PCIE SPEC
VCC3:3A
12V:5.5A
3VSB:0.375A



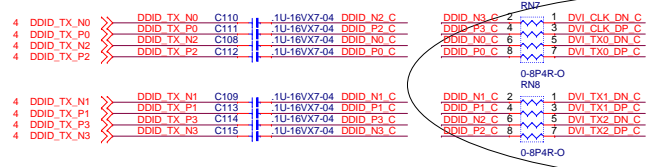
Between PCIe16 & PCIe1

報價先上, 作Bom拿掉-Anthony

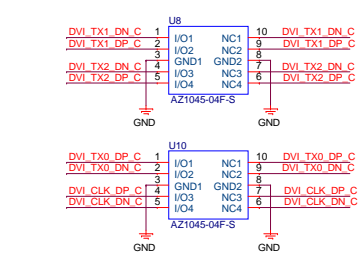
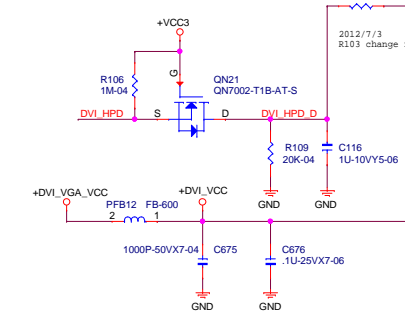
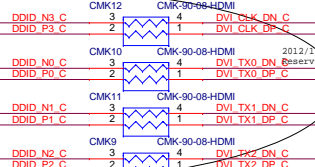
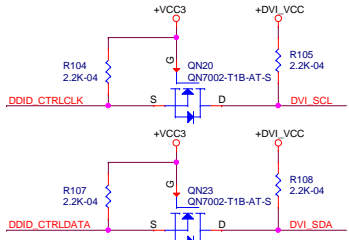
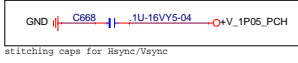


2013/6/11 Wilson
Add TACH5 for GPIO reset

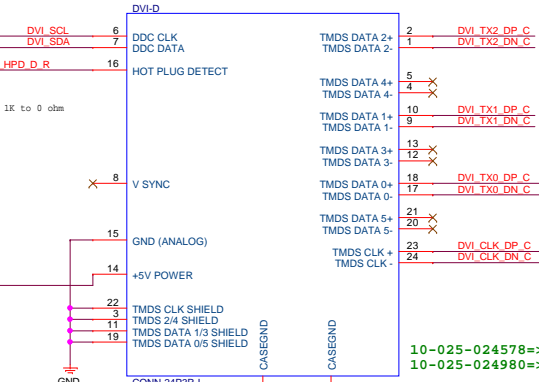
2012/7/05
PCIe Gen3 slot reset circuit update .



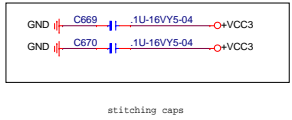
2013/2/26 Wilson: Change Res array to 470ohm



for EMI reserve



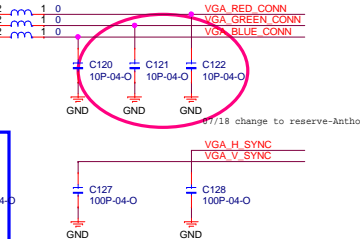
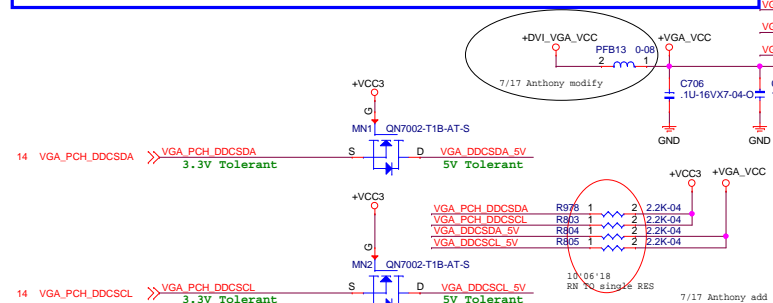
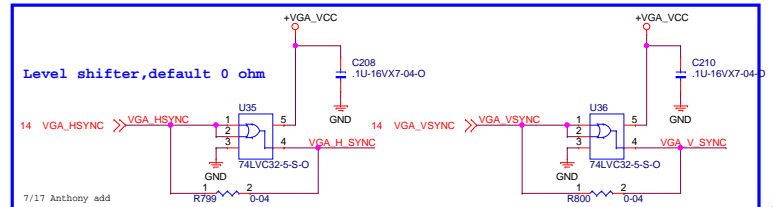
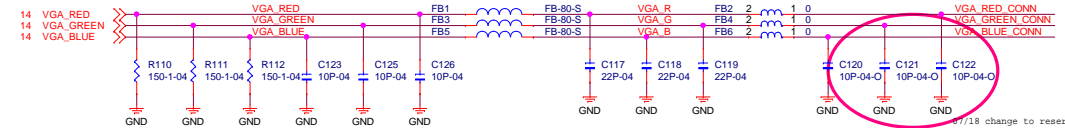
10-025-024578=>一般DVI port
10-025-024980=>多4個固定腳DVI



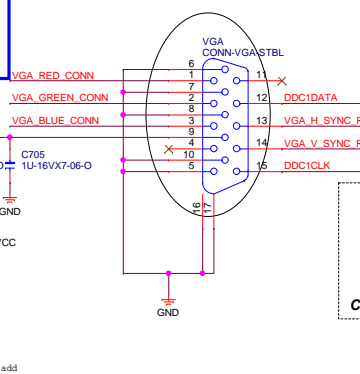
stitching caps

DVI-D

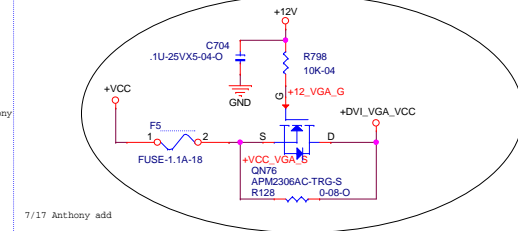
VGA



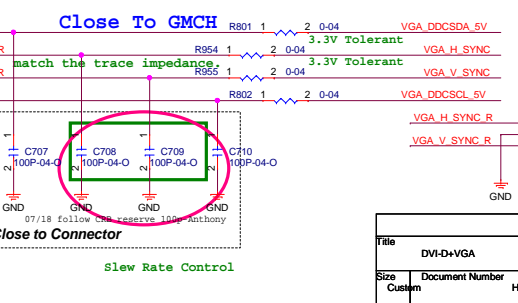
2013/1/23 Wilson: change VGA to standard



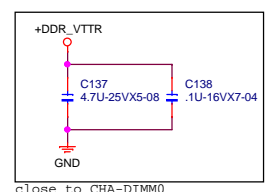
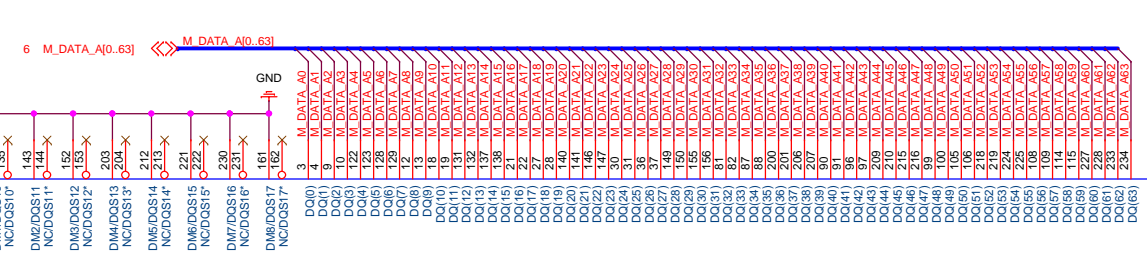
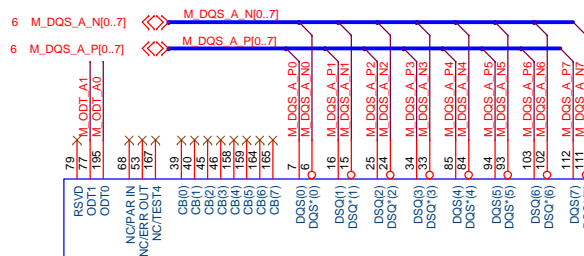
If build in Internal DVI Con, that can use the circuit to protect reverse voltage together.



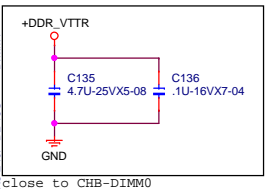
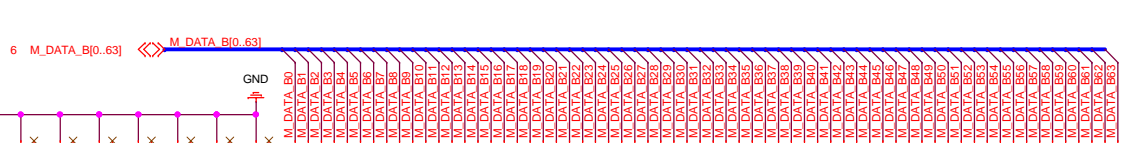
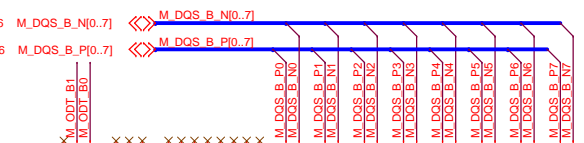
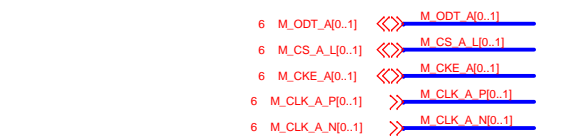
7/17 Anthony add



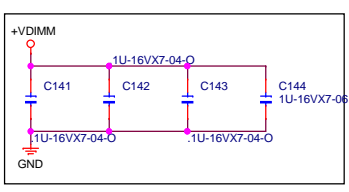
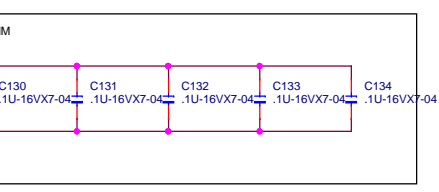
Title	DVI-D+VGA
Size	Custom
Document Number	H81H3-AM
Date	Friday, June 21, 2013
Sheet	10 of 39
Rev	1.0



CHANNEL A DIMMs

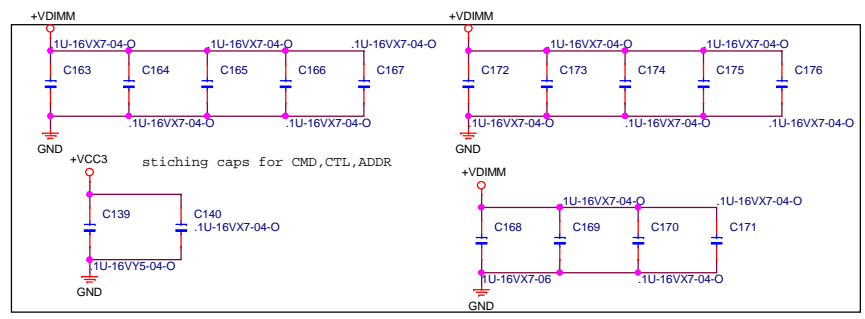


CHANNEL B DIMMs



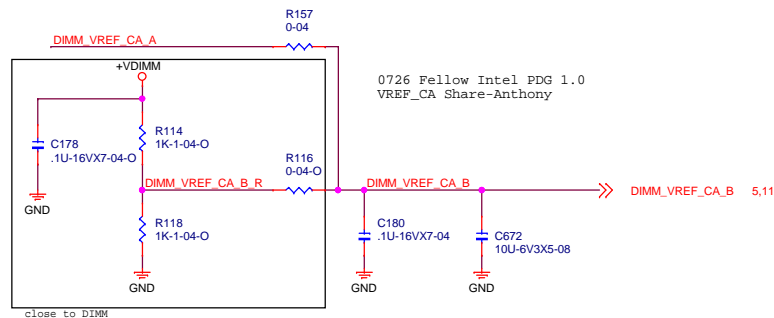
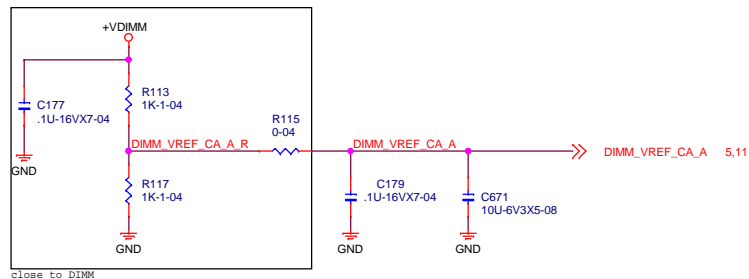
close to CHA-DIMM2

close to CHB-DIMM1

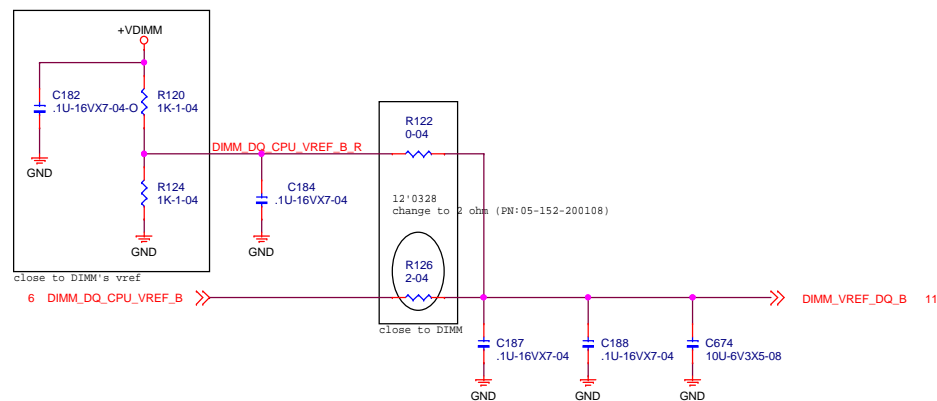
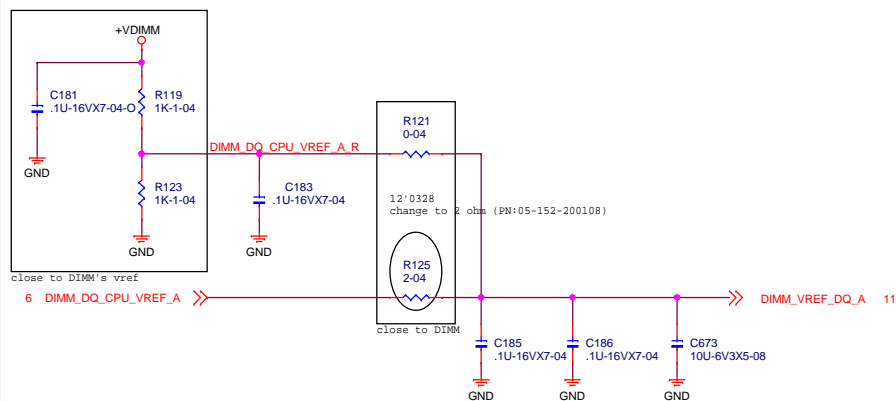


place between CHA&CHB
Don't punch VIAS

DDR3-CHA			
Size	Document Number	Rev	
Custom	H81H3-AM	1.0	
Date:	Friday, June 21, 2013	Sheet	11 of 39



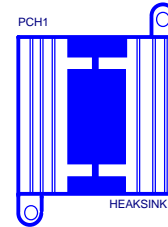
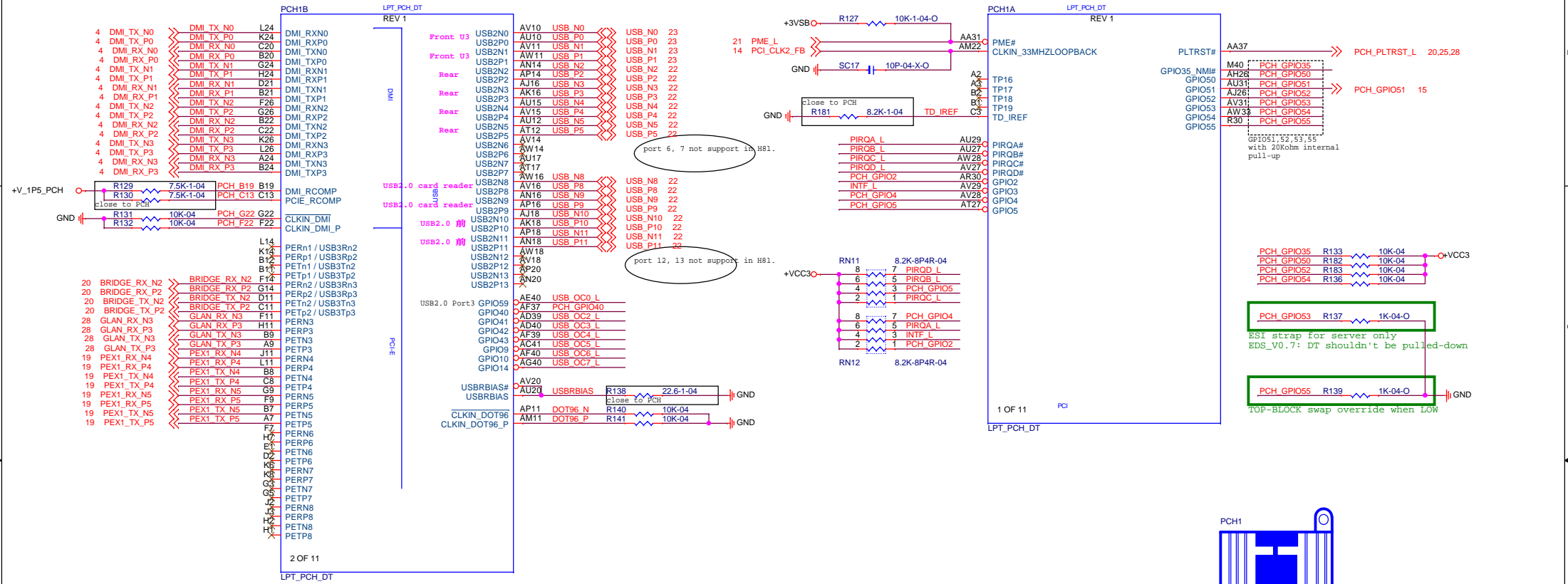
DIMM_VREF_CA Circuit



DIMM_VREF_DQ Circuit

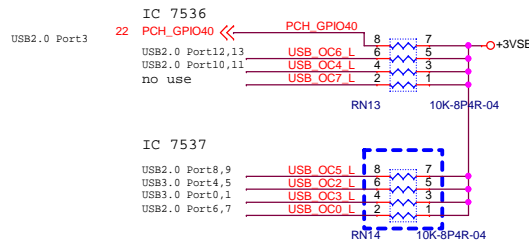
GND C857 1U-16VY5-04-0 +V_1P05_PCH

stitching caps for DMI

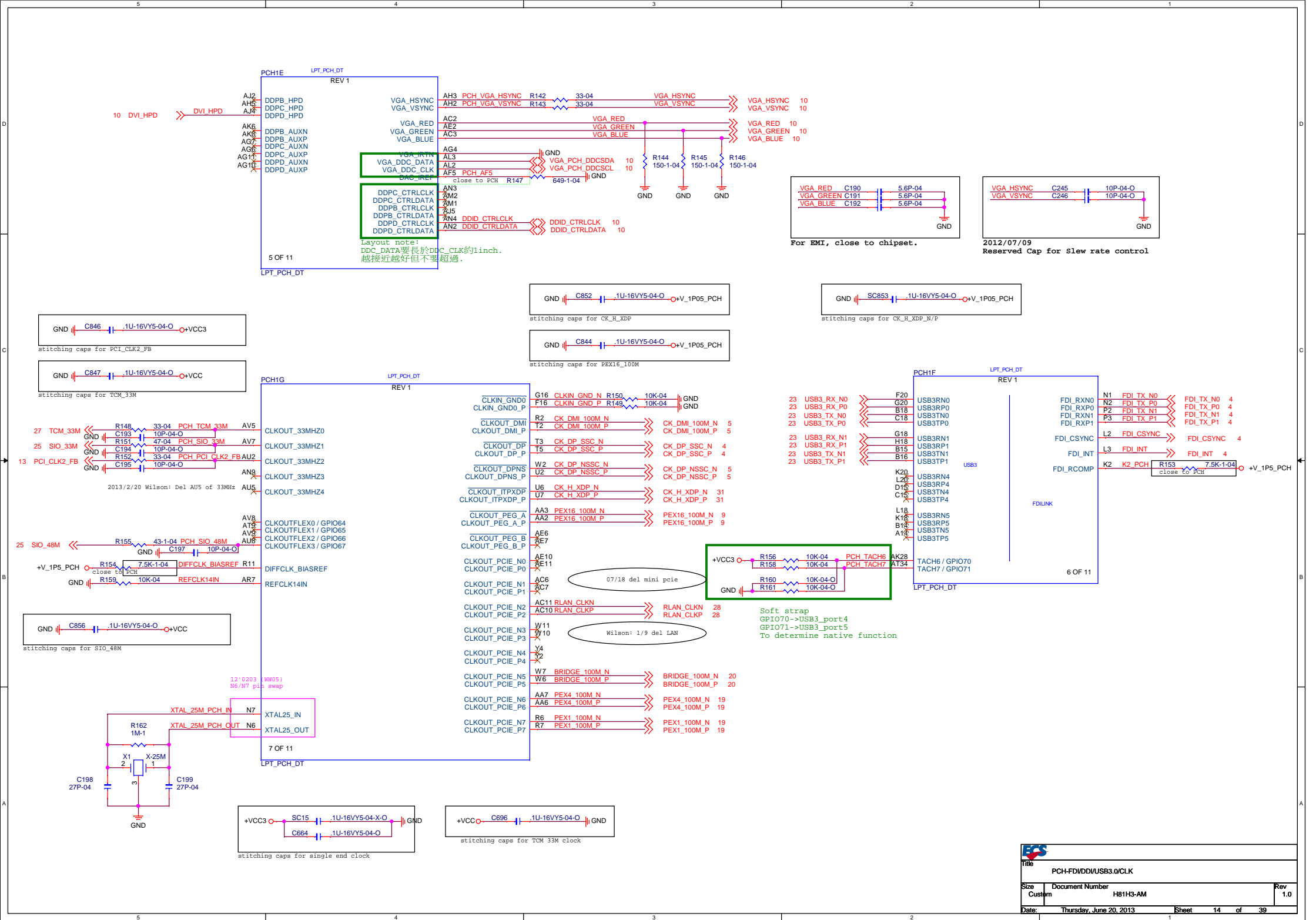


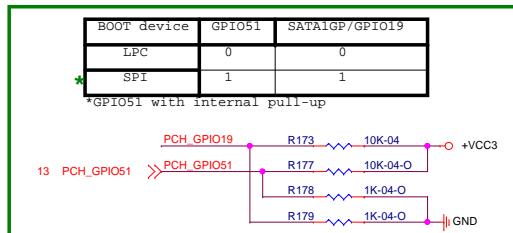
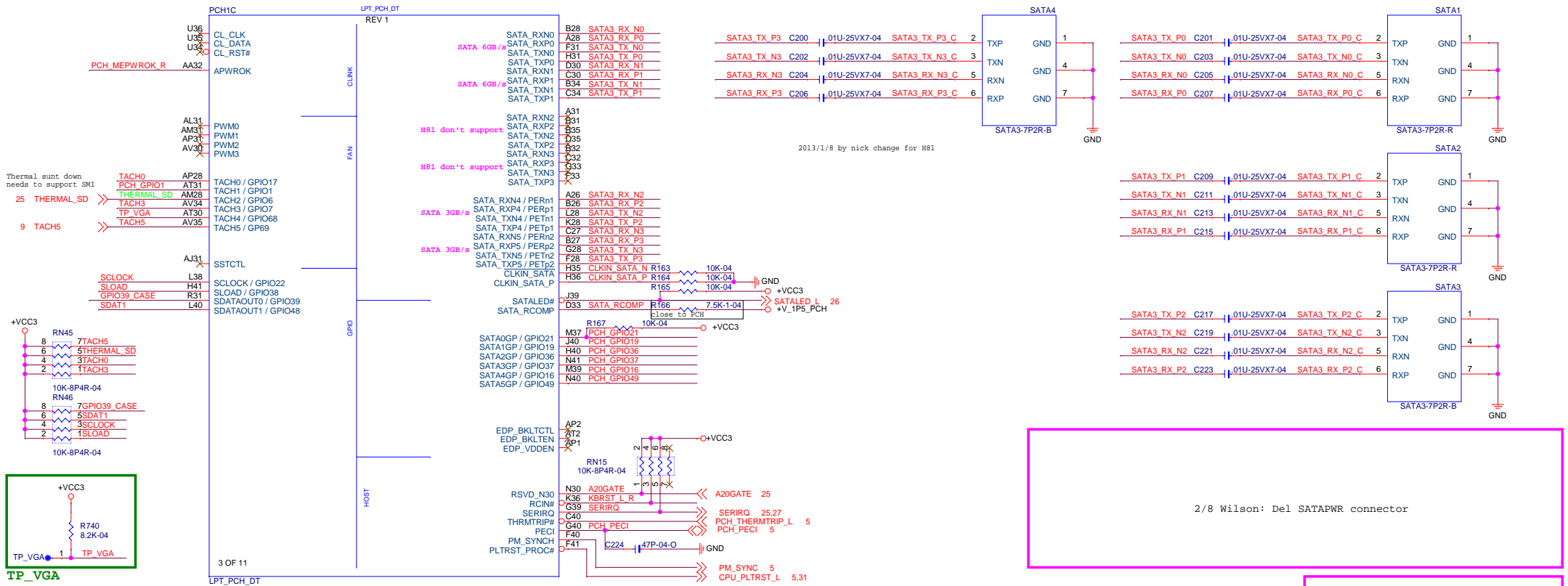
PCH heatsink (T/U phase)
P/N:20-120-014550
20-120-013505

PCH chipset (SMD)
P/N:01D201-082640

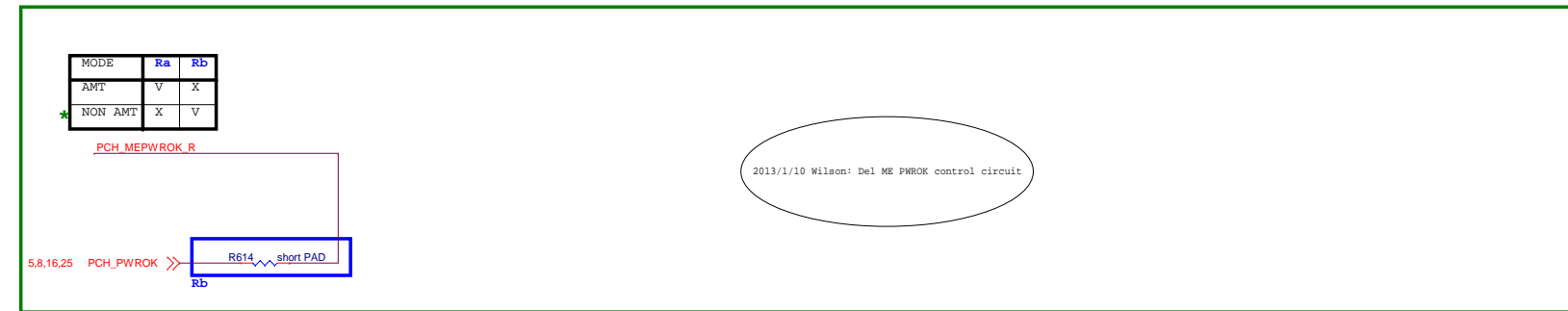
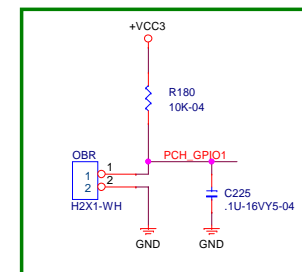
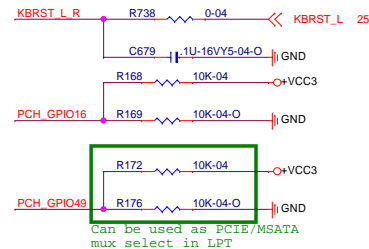
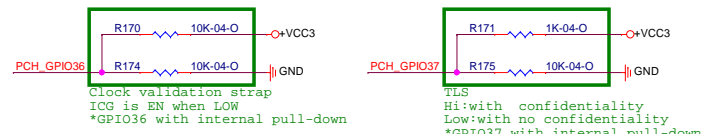


0727 If no use usb OC#
need pull up 3VSB by 10KΩ-Anthony

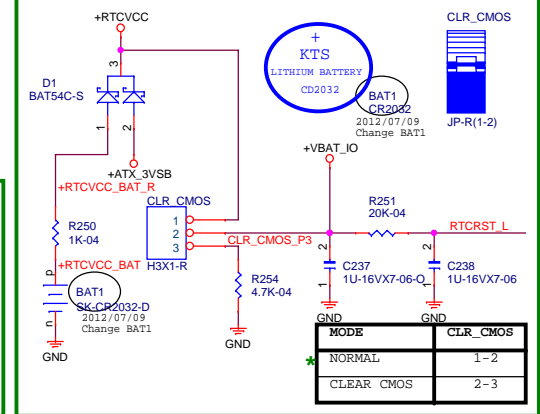
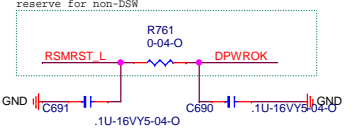
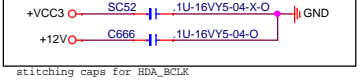
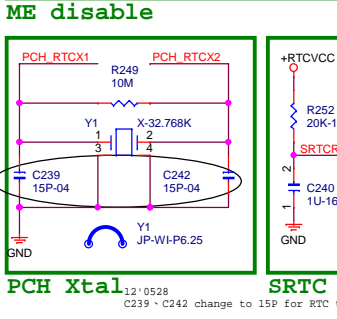
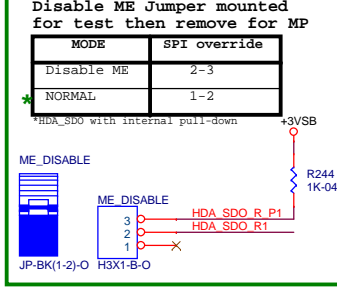
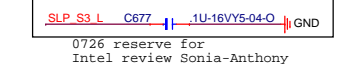
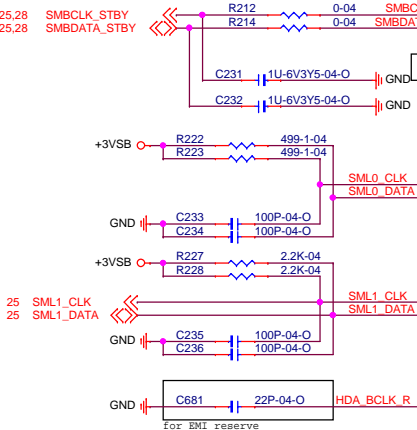
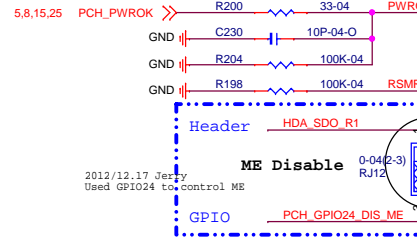
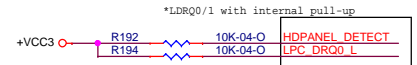




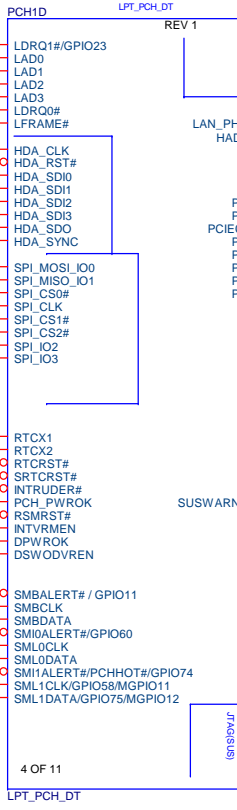
2013/1/21 Wilson: remove pull high resistor



ME PWROK control circuit



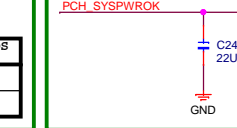
CLR CMOS



4 OF 11

2013/1/18 Wilson: Del reserve circuit

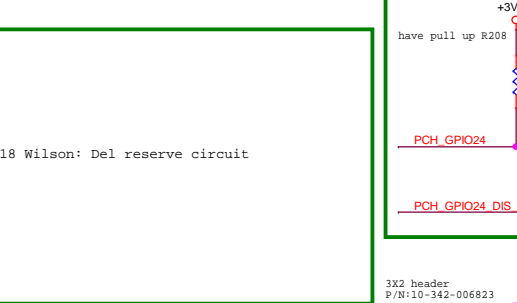
HSW Strap CFG13



Reserve for Debug



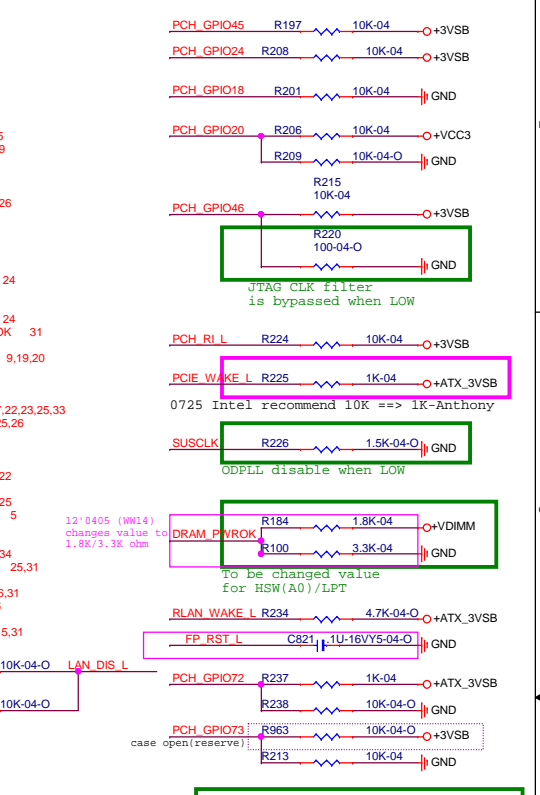
ME Disable



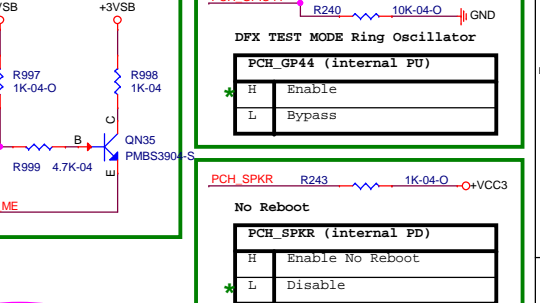
ME Test Header



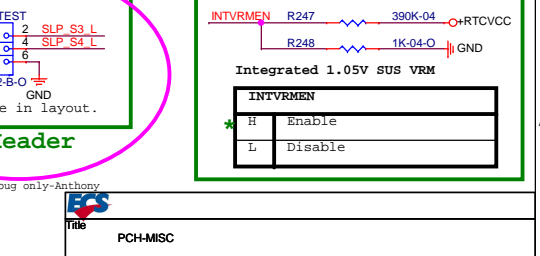
Reserve for Debug



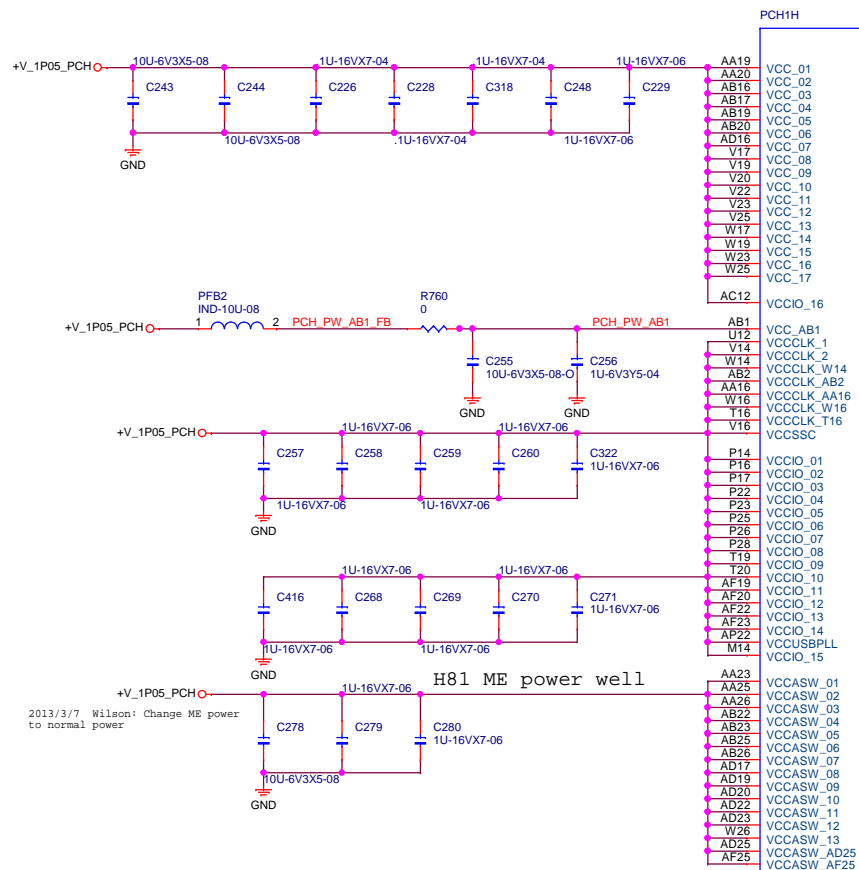
case open(reserve)



DFx TEST MODE Ring Oscillator



No Reboot



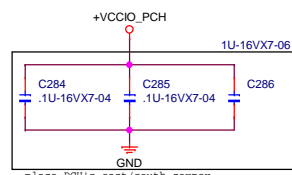
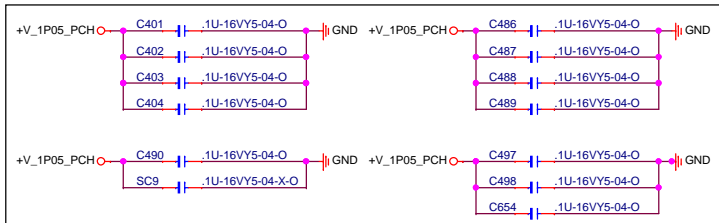
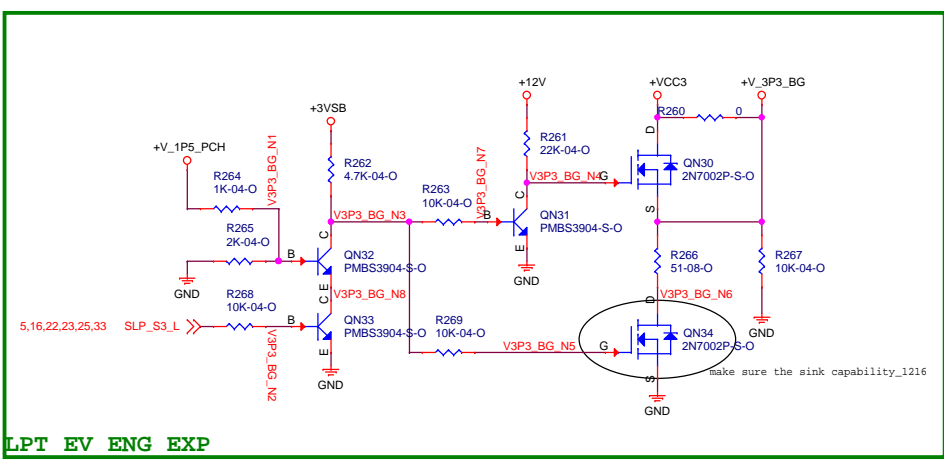
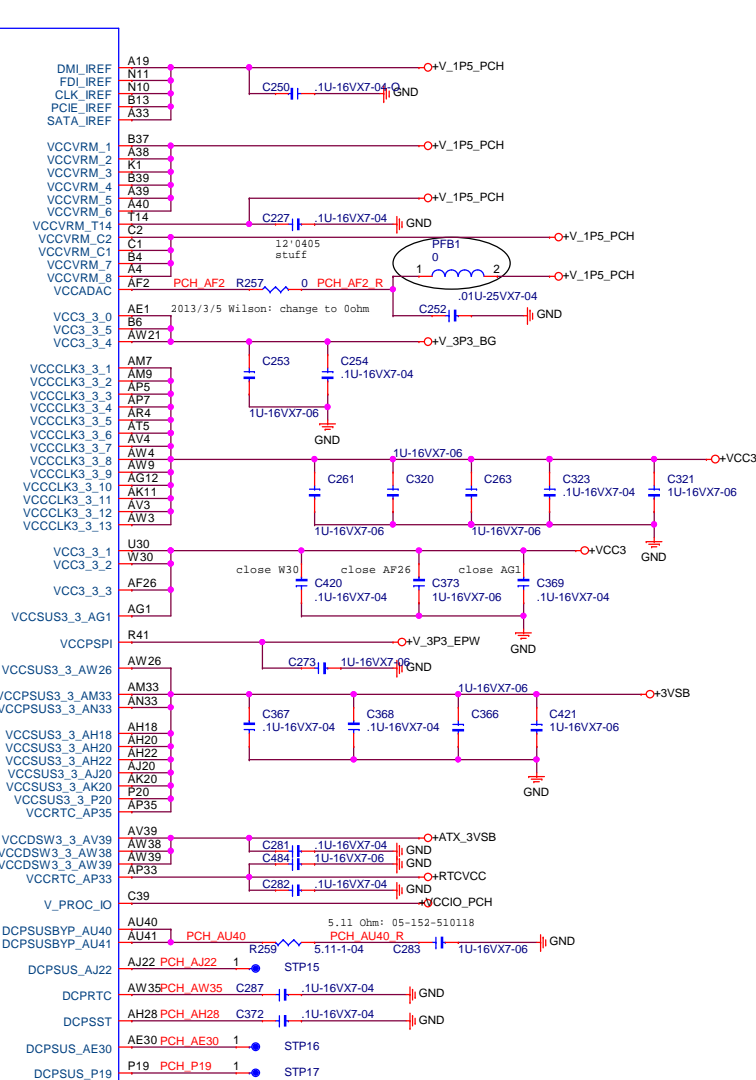
PCH1H

LPT_PCH_DT

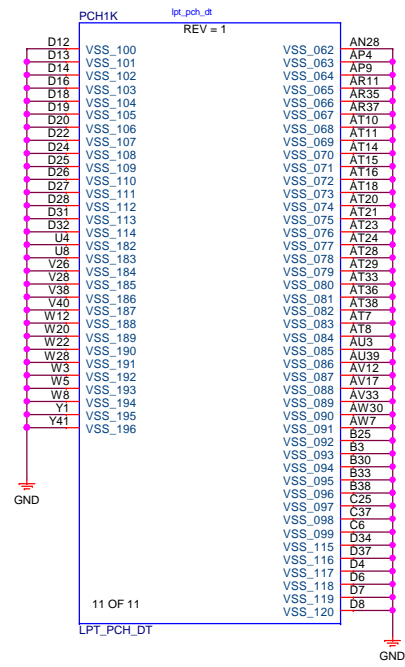
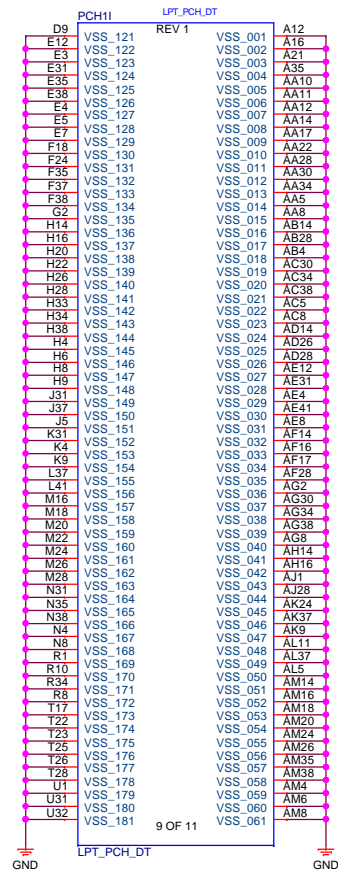
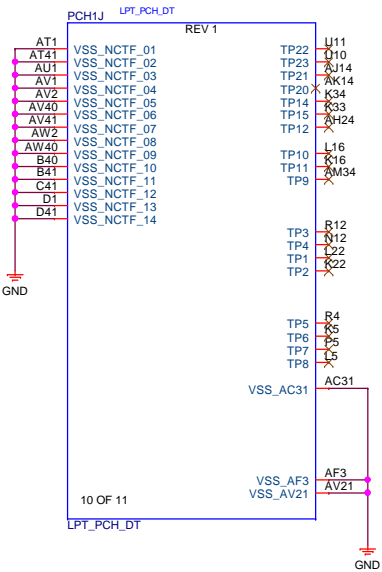
REV 1

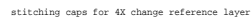
8 OF 11

LPT_PCH_DT

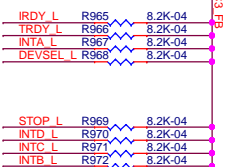
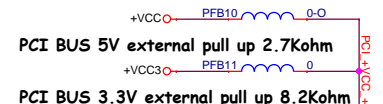
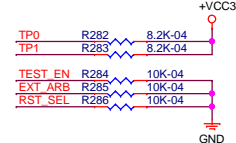
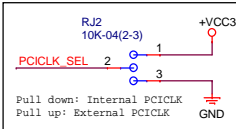
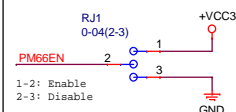
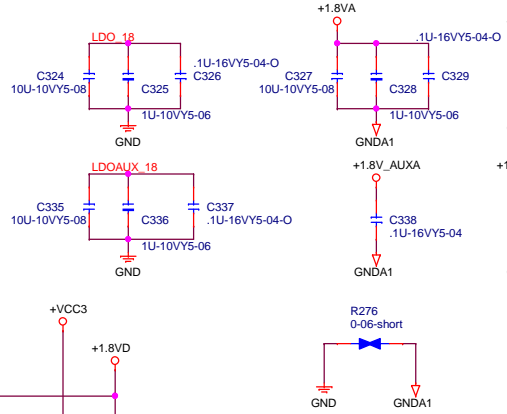
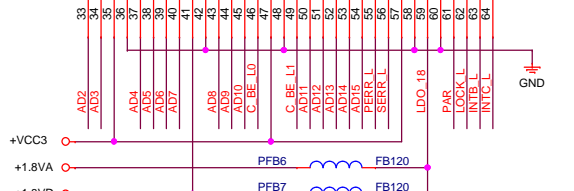
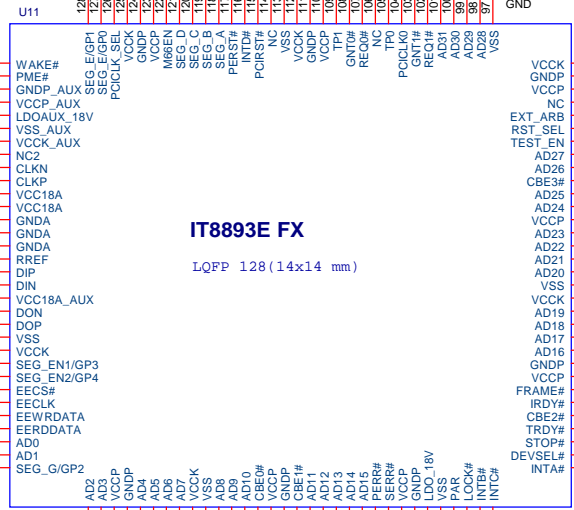
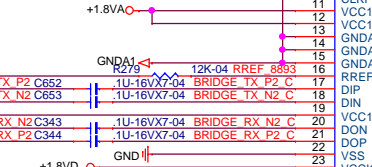
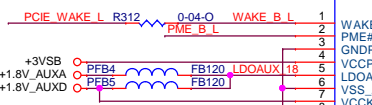
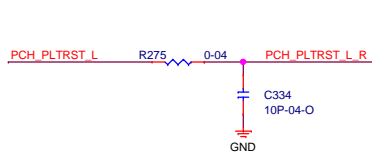
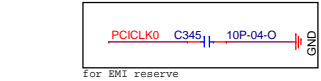
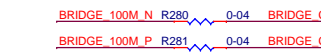
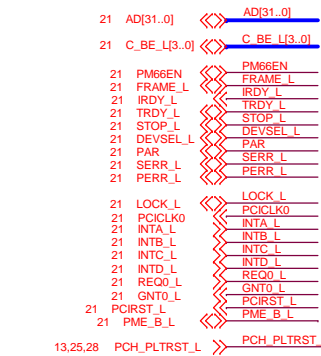


Title			
PCH-POWER			
Size	Document Number	Rev	
Custom	H81H3-AM	1.0	
Date:	Thursday, June 20, 2013	Sheet	17 of 39





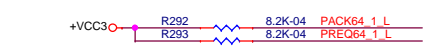
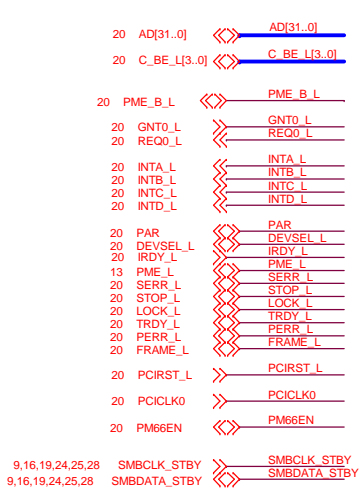
報價先上,作Bom拿掉-Anthony



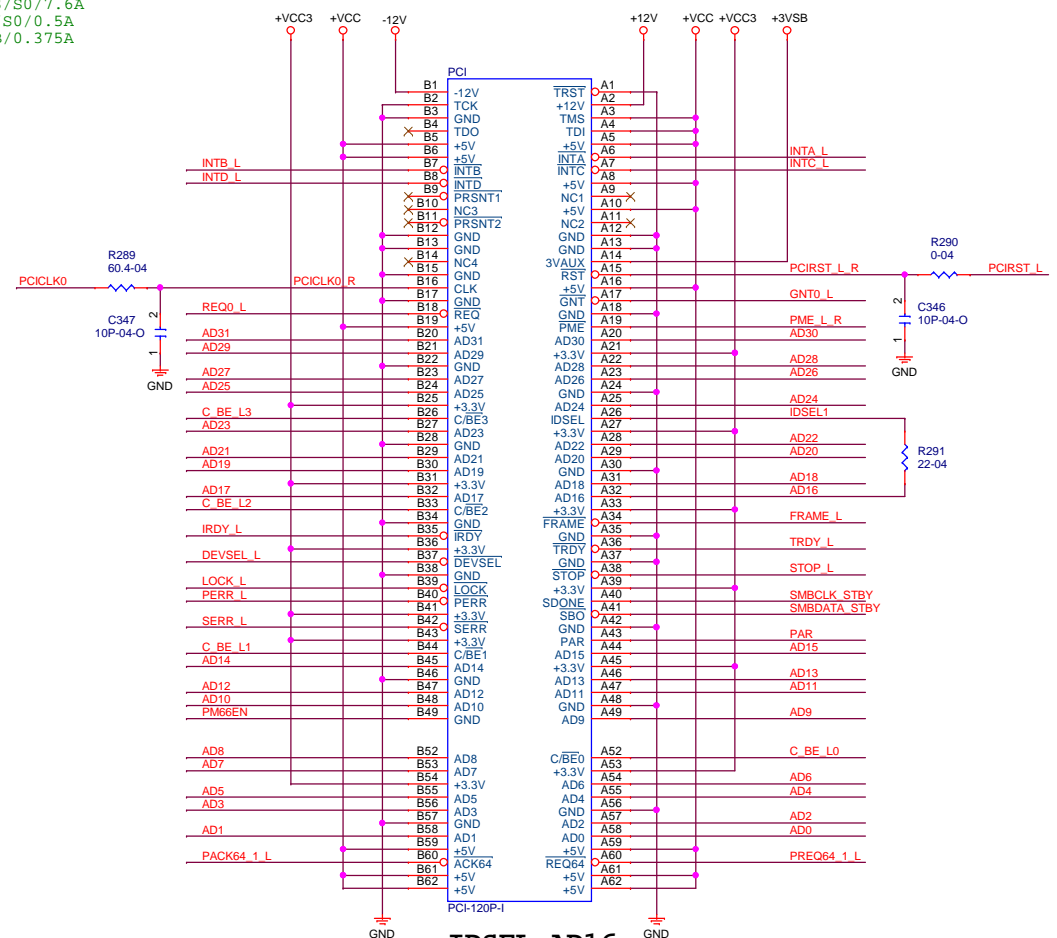
0726 Add pull up for ITE review-Anthony

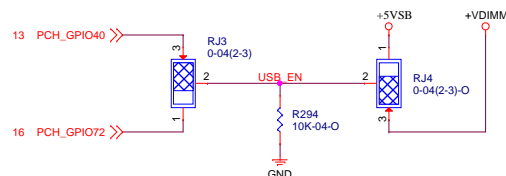
PCIE CLK PCB layout note:
To meet Differential Impedance :100 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
CLKP and CLKN trace width:7 mils
Space between CLKP and CLKN:14 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 4 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inches (Max.)
The size of R4;R5 is "0402"
The size of R6;R7 is "0402"

PCIE DIP;DIN;DOP;DON PCB layout note:
To meet Differential Impedance :85 ohm +/- 15%
To meet Single-ended Impedance :50 ohm +/- 15%
PCIE DIP and DIN trace width:9.5 mils
PCIE DOP and DON trace width:9.5 mils
Space between DIP/DIN and DOP/DON:14.5 mils
L1 & L2 height:5 mils
The signal traces Number of vias: 2 (Max.)
The signal trace above analog GND plane
Spacing from other groups:>25 mils
Total trace length: 12 inches (Max.)
The size of C24;C25 is "0402"

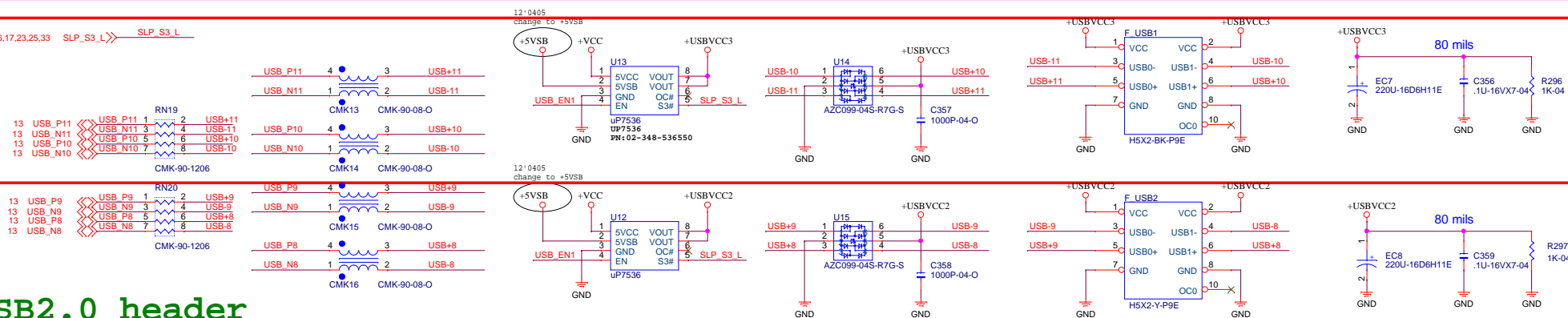
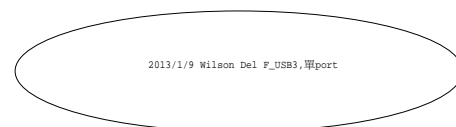
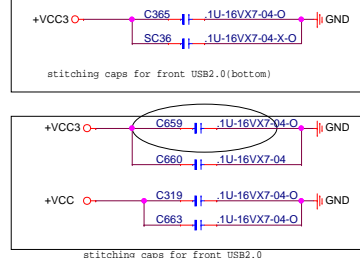


PCI Slot
+VCC/S0/5A
+VCC3/S0/7.6A
+V12/S0/0.5A
+3VSB/0.375A

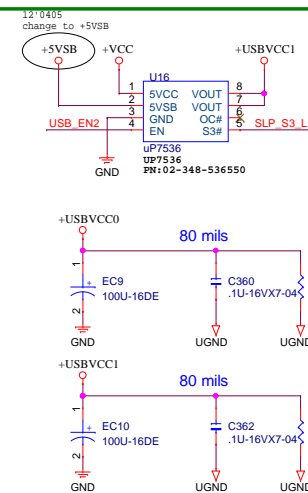
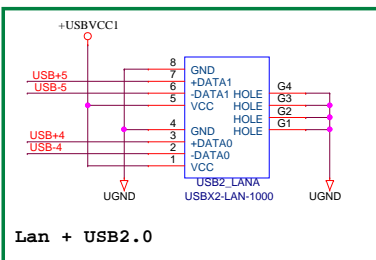
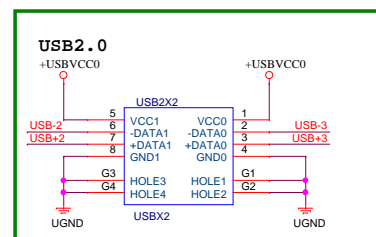
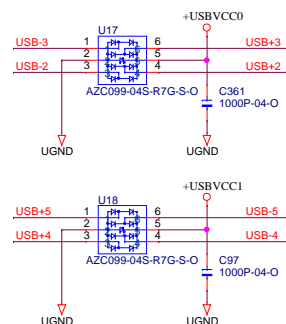
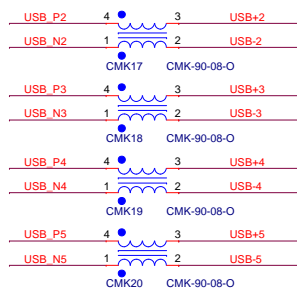
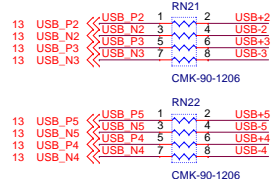




	uP7536 Enable use	RJ?	RJ?	S4/S5 USB_5V_DUAL	Customer
	VDIMM	0ohm (1-2)	NA	0 Volt	Acer S4 w/o S5 w/ USB_5VDUAL
	5VSB	0ohm (2-3)	NA	5 Volt	
*	GPIO	NA	0 ohm	S4 : 0 Volt S5 : 5 Volt	

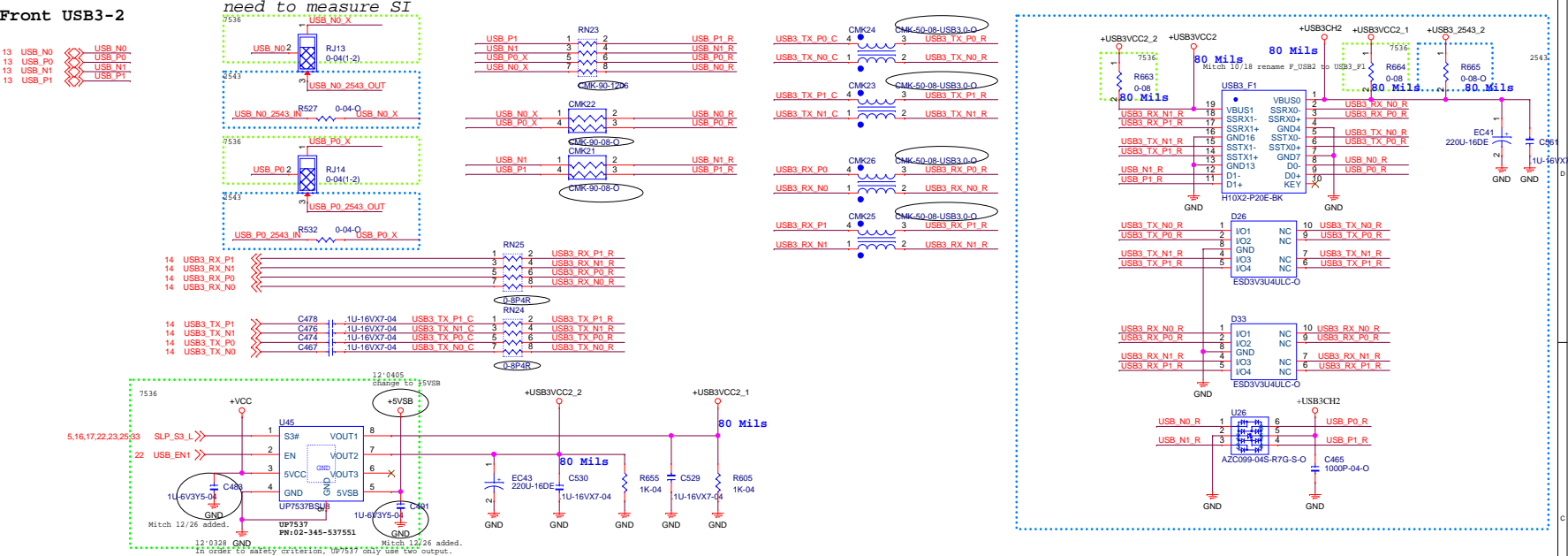
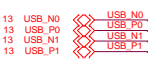


USB2.0 connector

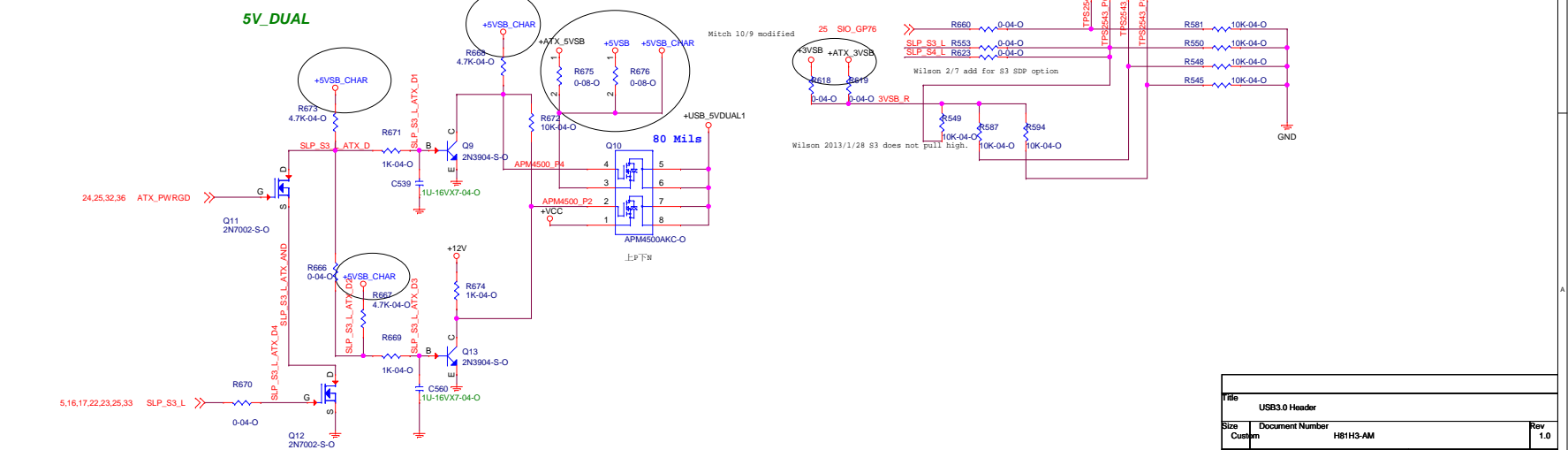


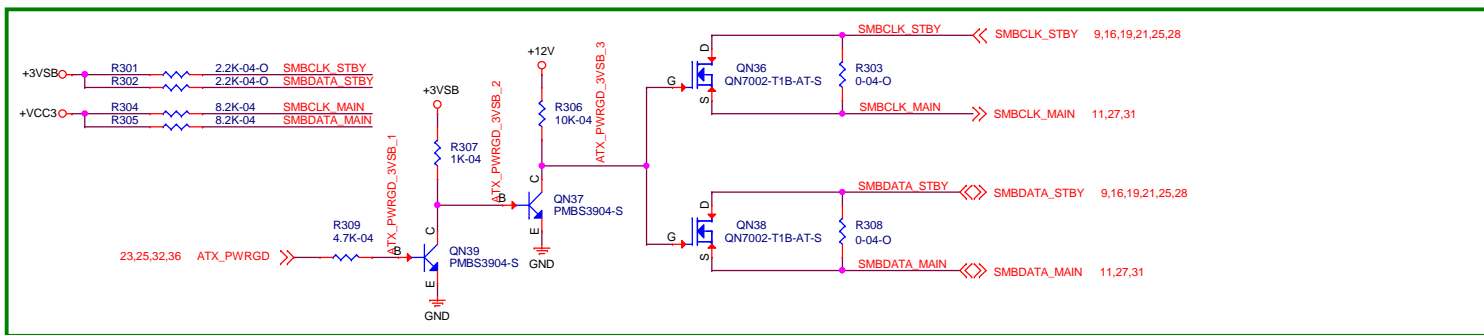
3. OC[3:0]# should be connected with USB 2.0 ports 0 - 7 and any 4 of USB 3.0 ports 1 - 6.
4. OC[7:4]# should be connected with USB 2.0 ports 8 - 13 and any 4 of USB 3.0 ports 1 - 6.

Front USB3-2

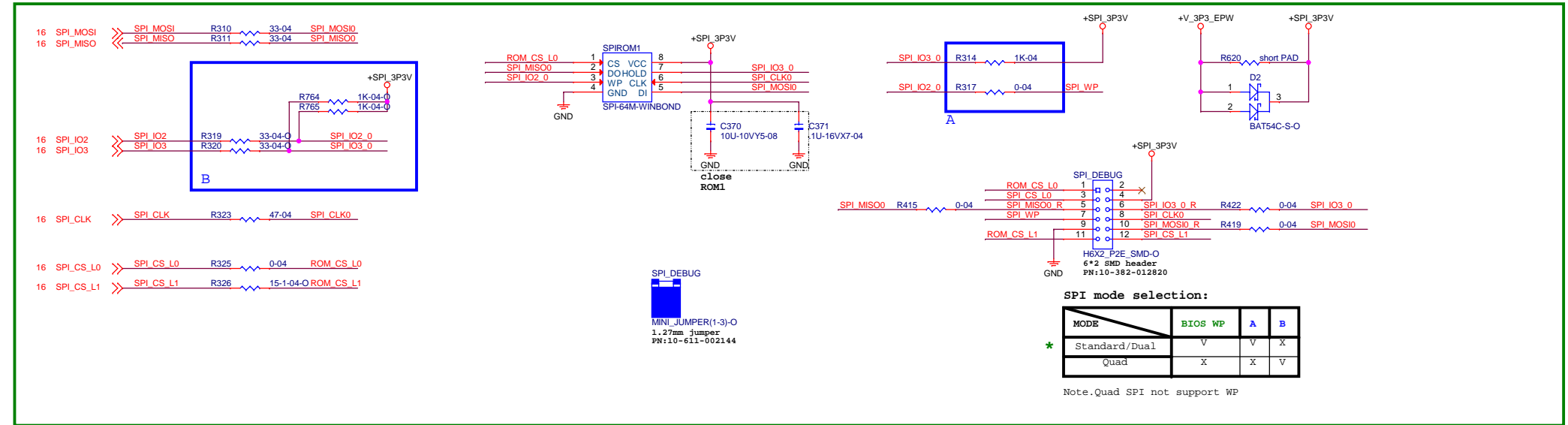


Input Logic Level				Logic Output	
INPUT1	INPUT2	INPUT3	ILIM_SEL	2543	
S4	Pull High	Pull High	S3	Charging Mode	WAKE Output (active low)
0	0	0	X	OUT discharge, power switch off	off
0	0	1	0	Dedicated charging port, auto-detect	off
0	1	0	X	Dedicated charging port, auto-detect, w/ Mouse/Keyboard detect + pass through enabled (back to auto detect when detached)	active low if DCP load present
X	1	0	X	Standard downstream port, USB 2.0 Mode	off
1	0	0	X	Dedicated charging port, BCL2 only	off
0	1	1	0	Auto mode, keyboard/mouse wakeup, no load detection	off
1	1	1	0	Standard downstream port, USB 2.0 Mode, no discharge	off
1	1	1	1	Charging downstream port, BCL2	active low if DCP load present

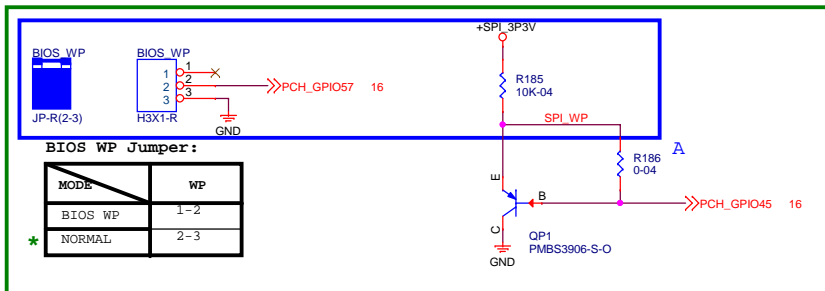




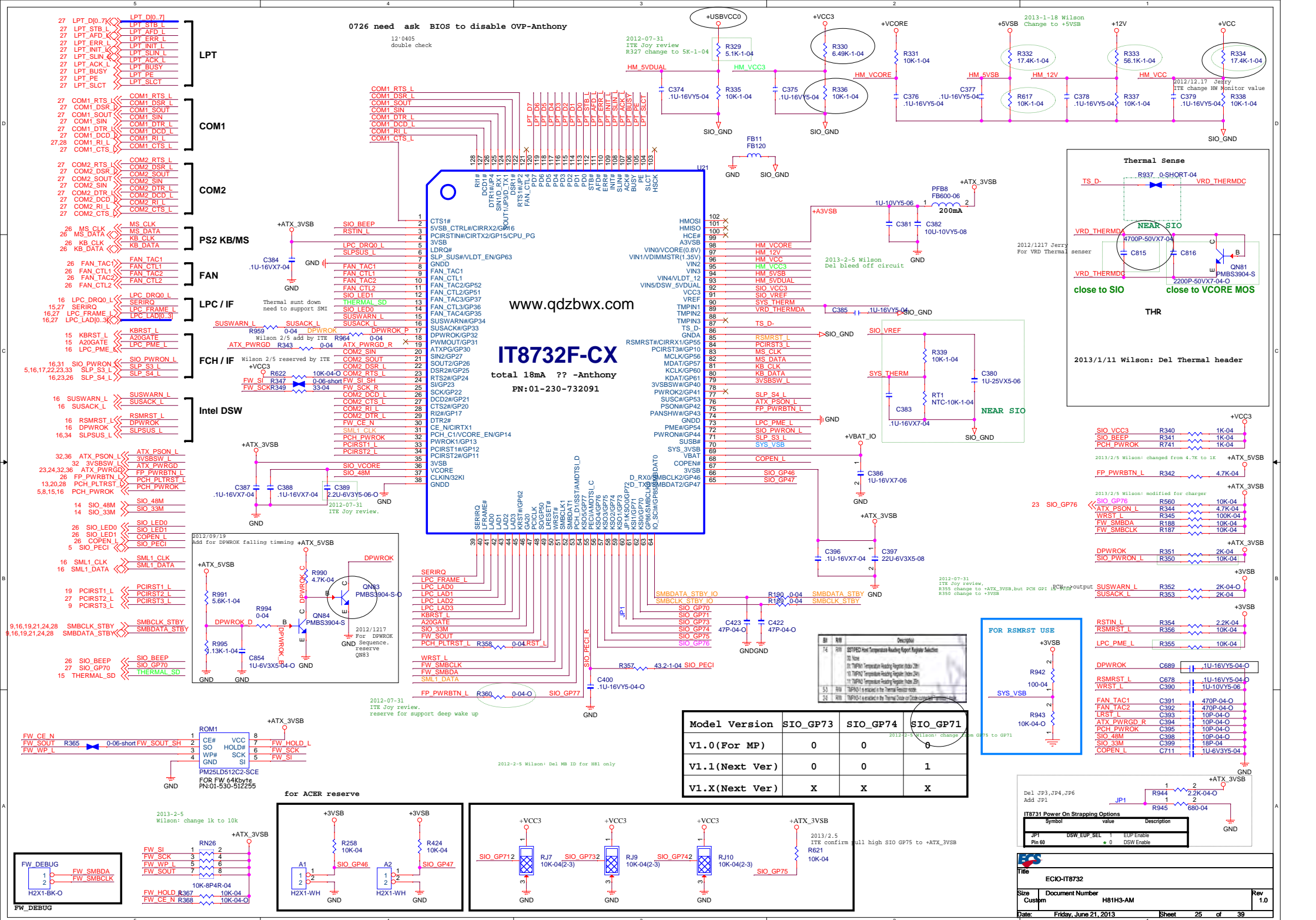
SMBus Logic Circuit

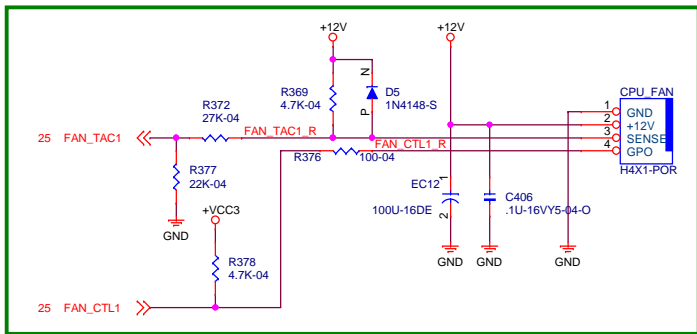


SPI ROM

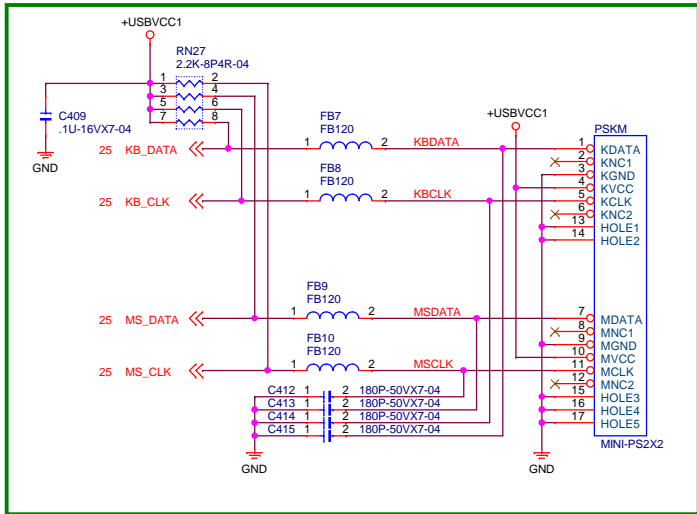


BIOS WP

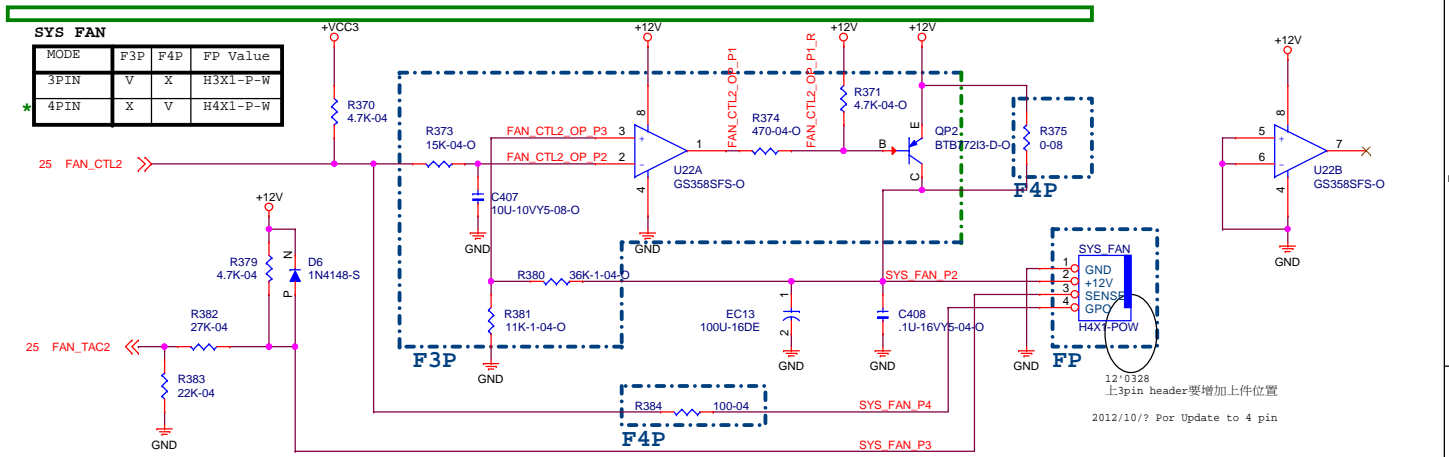




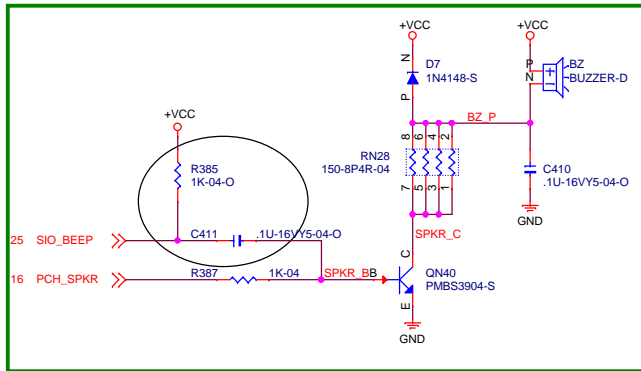
CPU_FAN 4 pin circuit

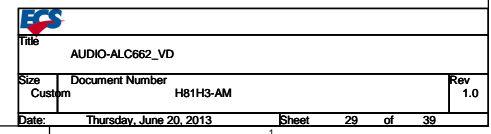
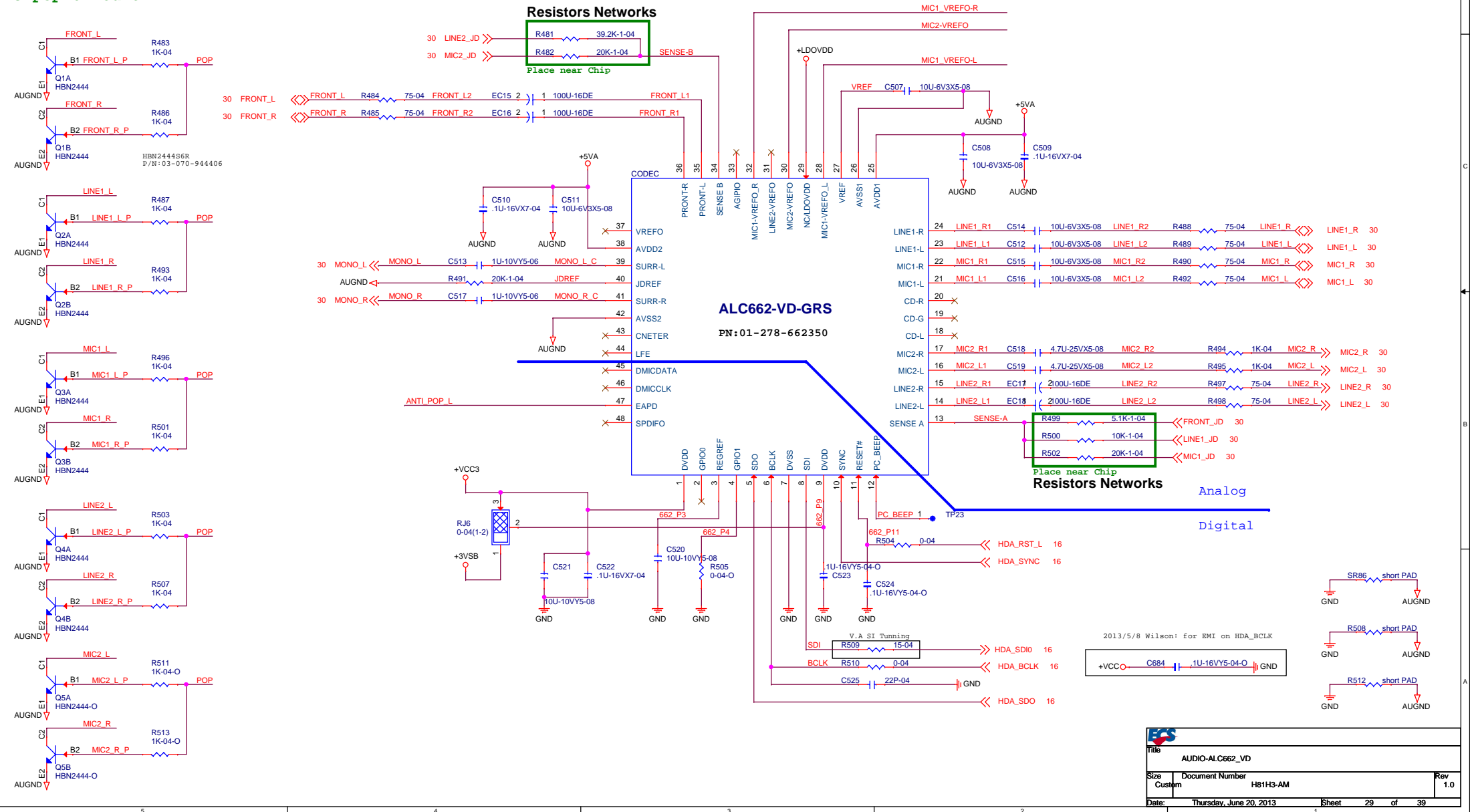
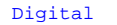
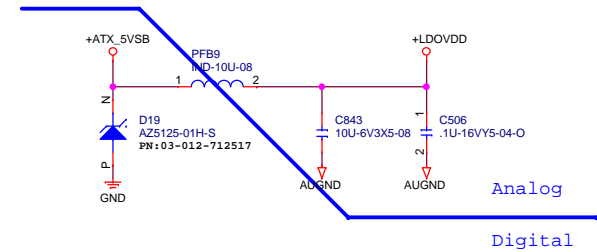
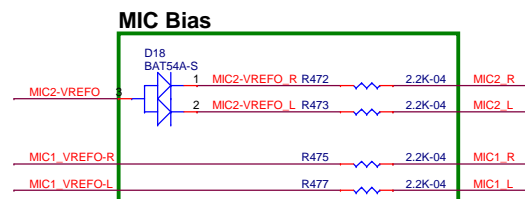
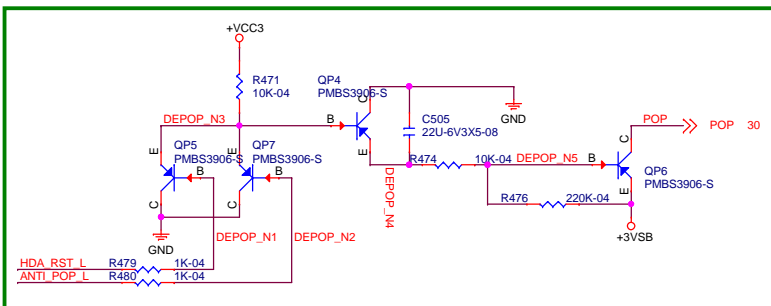


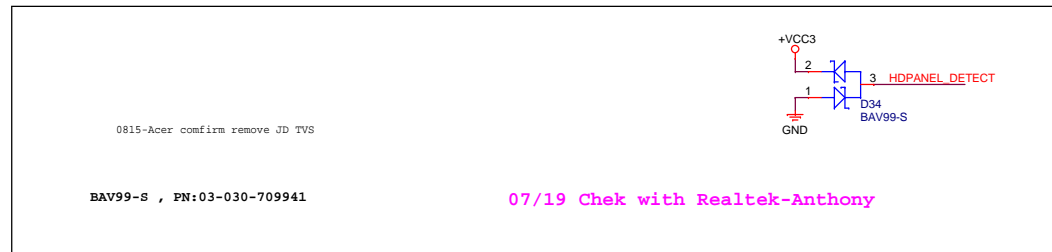
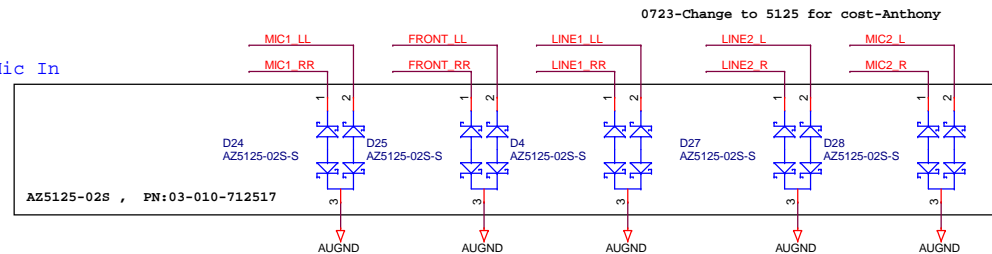
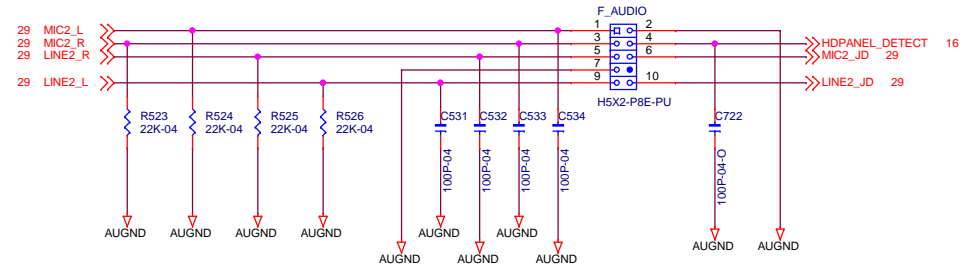
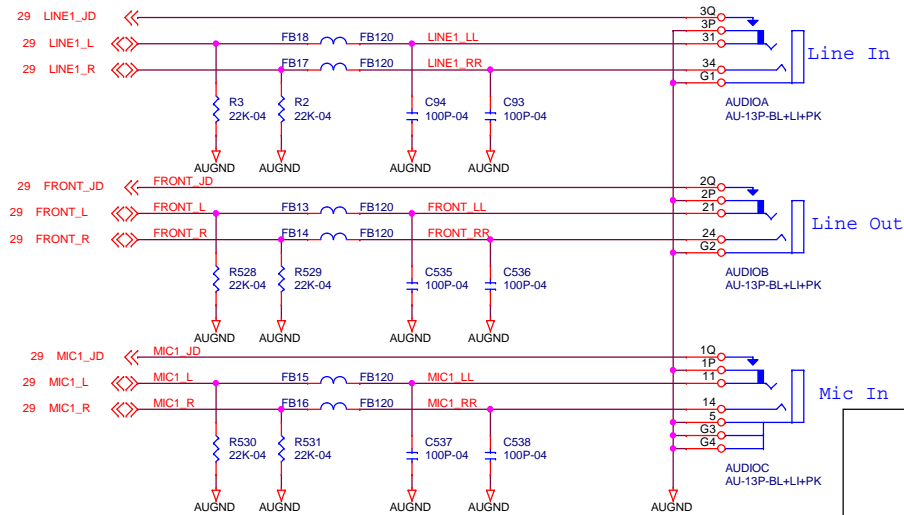
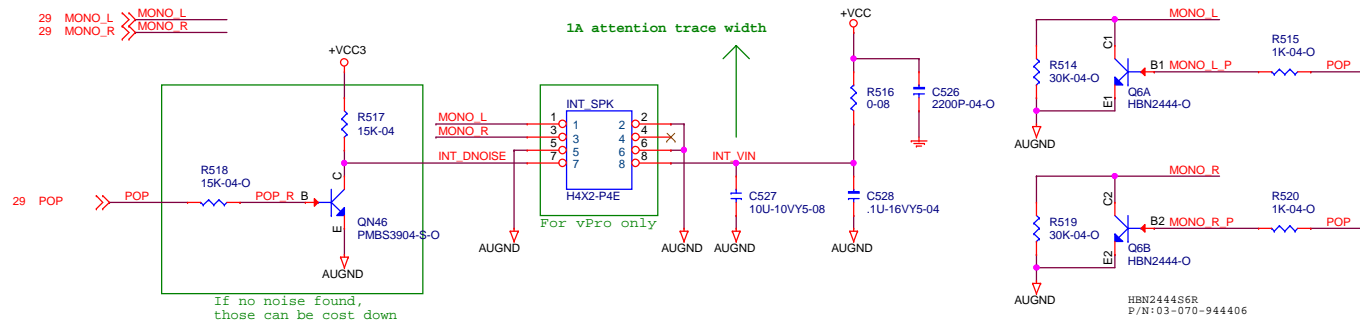
PS2 circuit

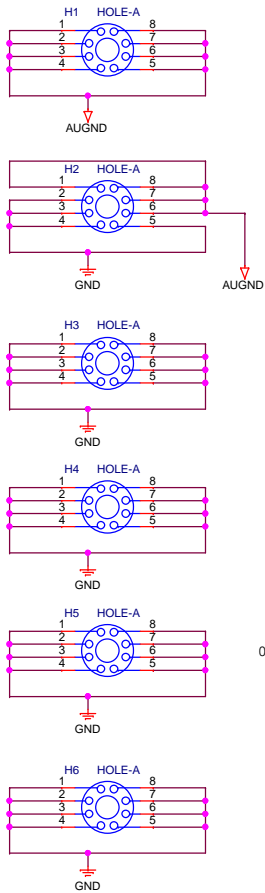


SYS_FAN 3/4 pin co-layout circuit

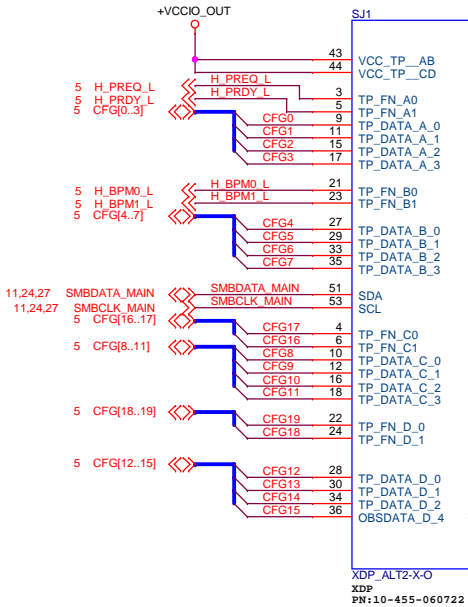




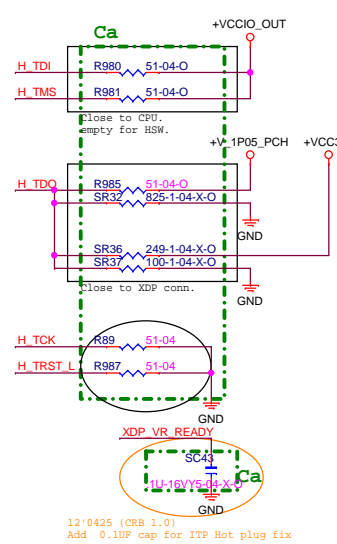
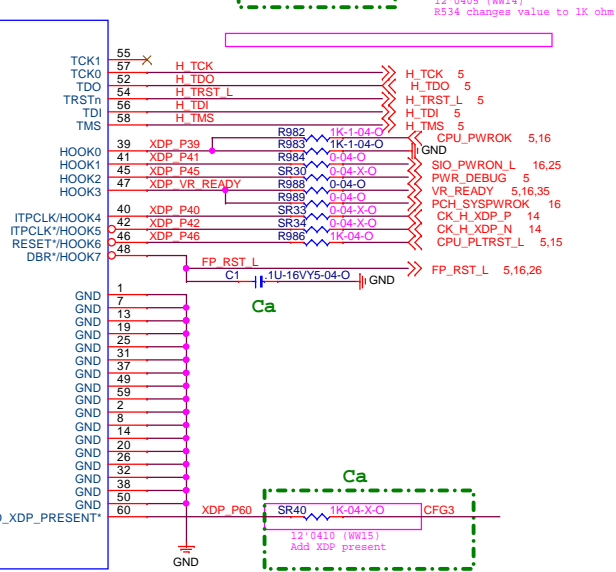




07/20 change to stuff for OC-Anthony

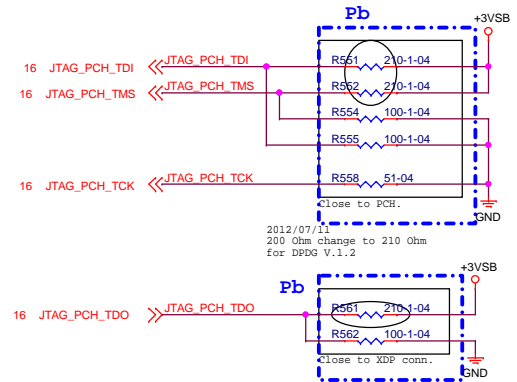


XDP
PN:10-455-060722



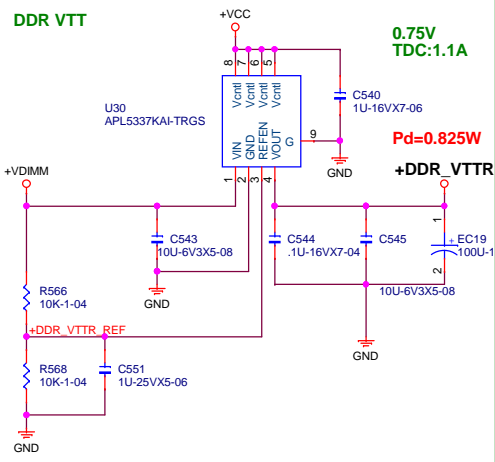
	Ca
CPU XDP function	V
NO CPU XDP function	X

-O:報價

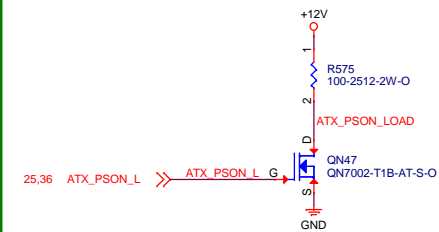


	Pb
PCH XDP function	V
NO PCH XDP function	X

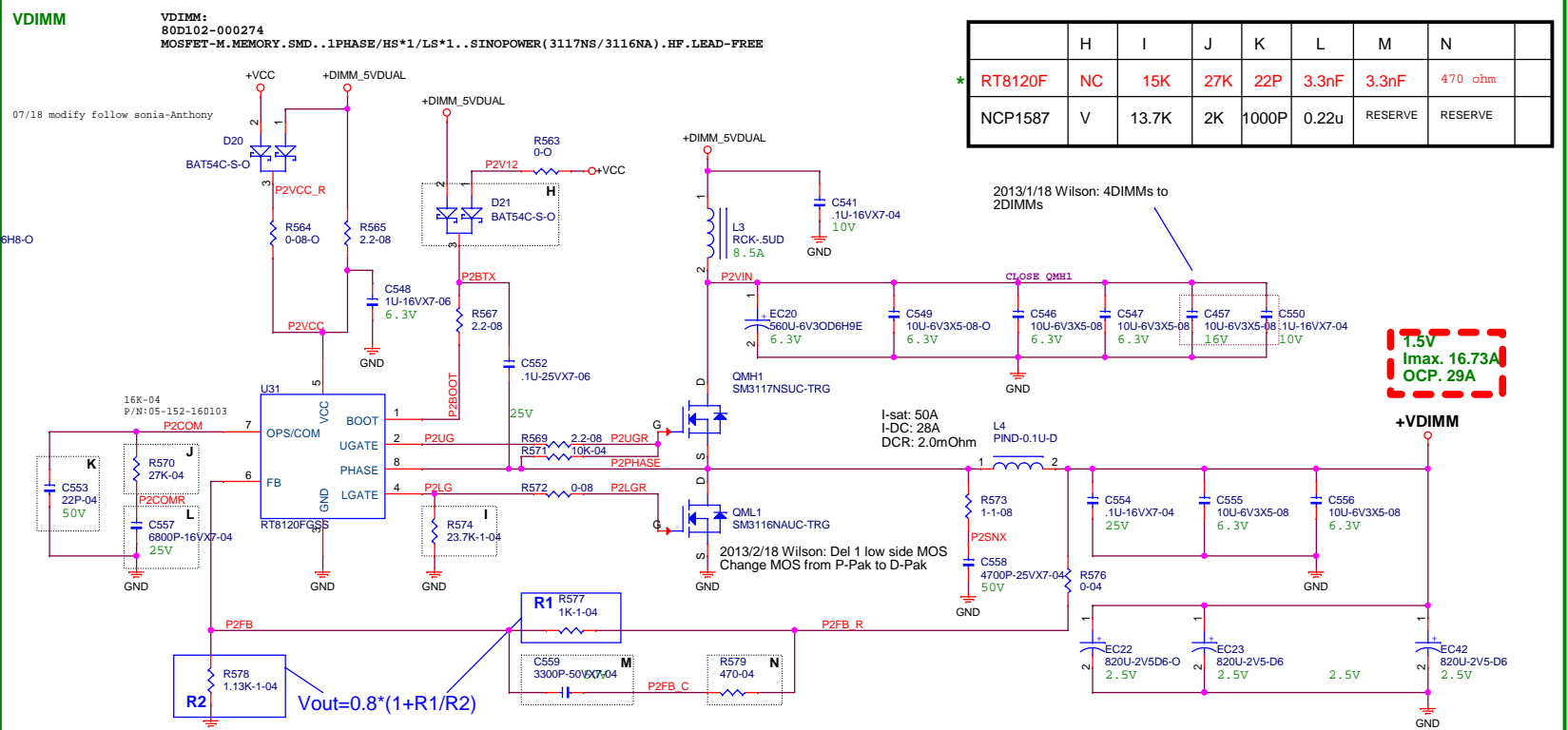
DDR VTT



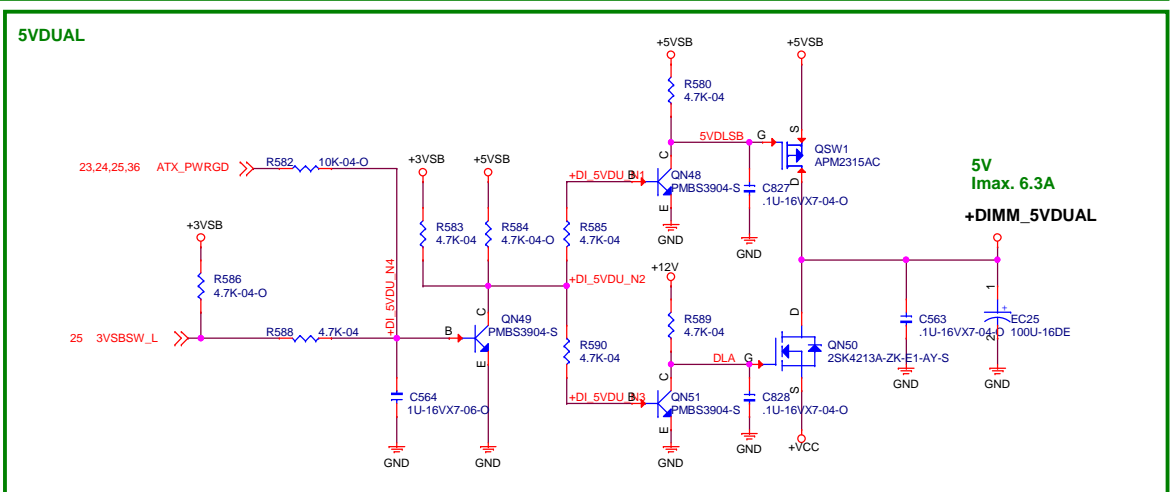
Dummy Load for ATX power



VDIMM

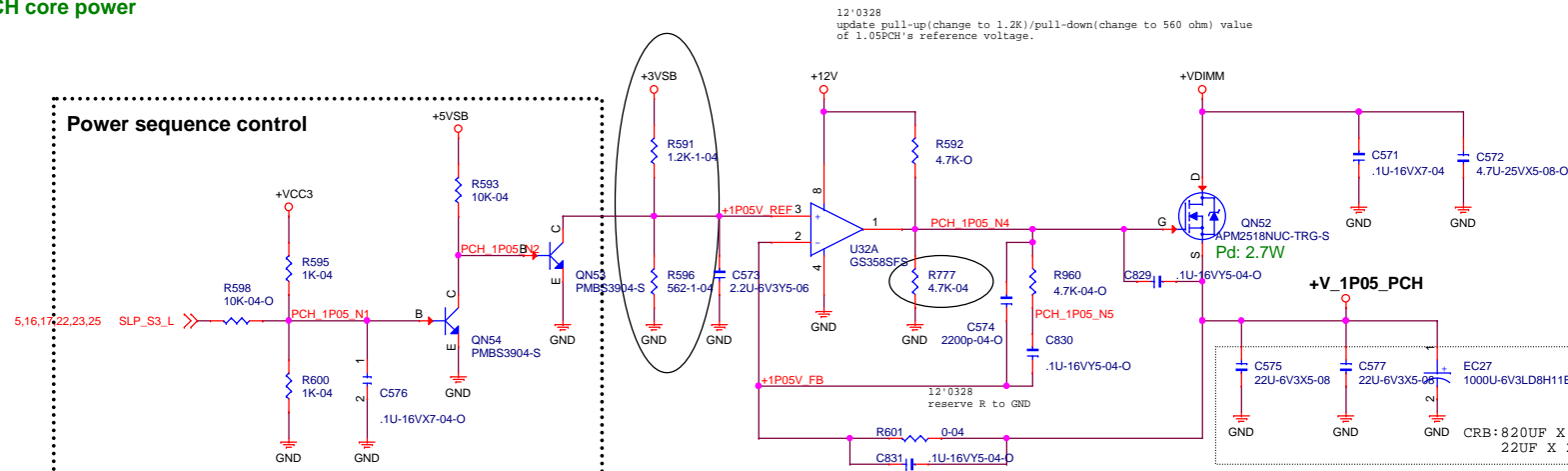


5VDUAL

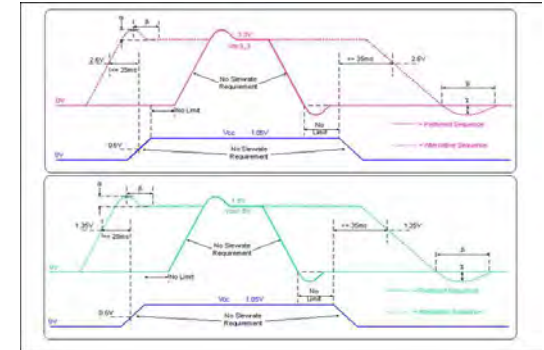
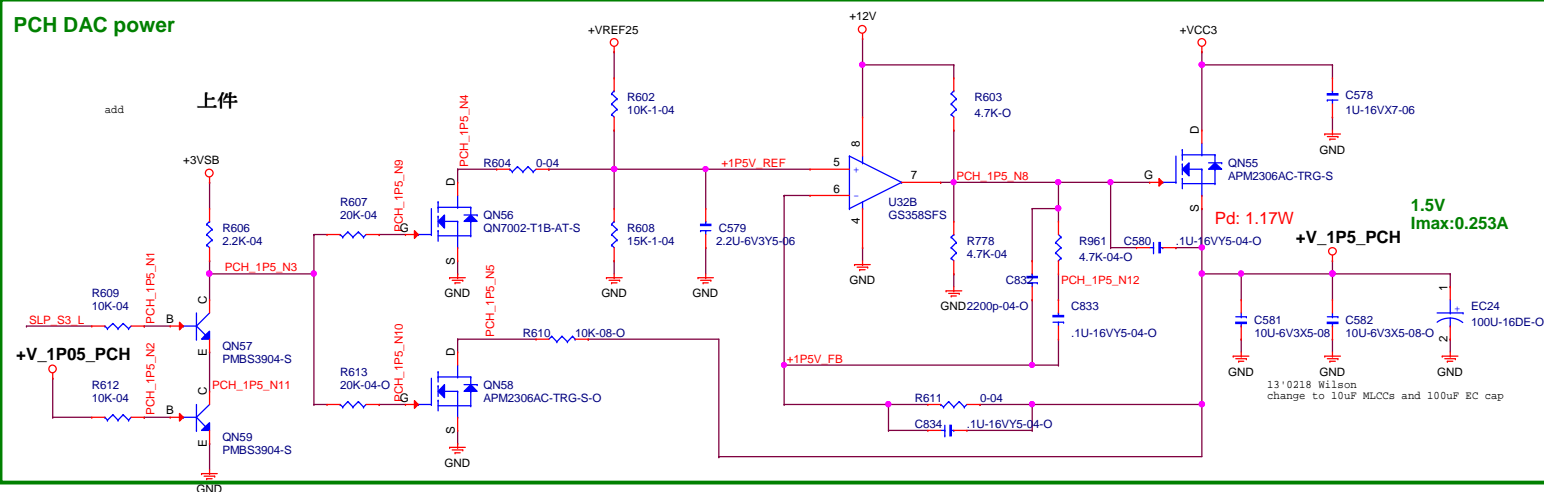


PCH core power

Power sequence control

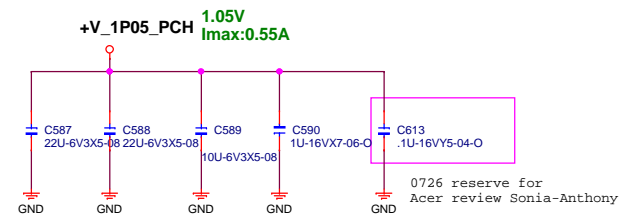


PCH DAC power

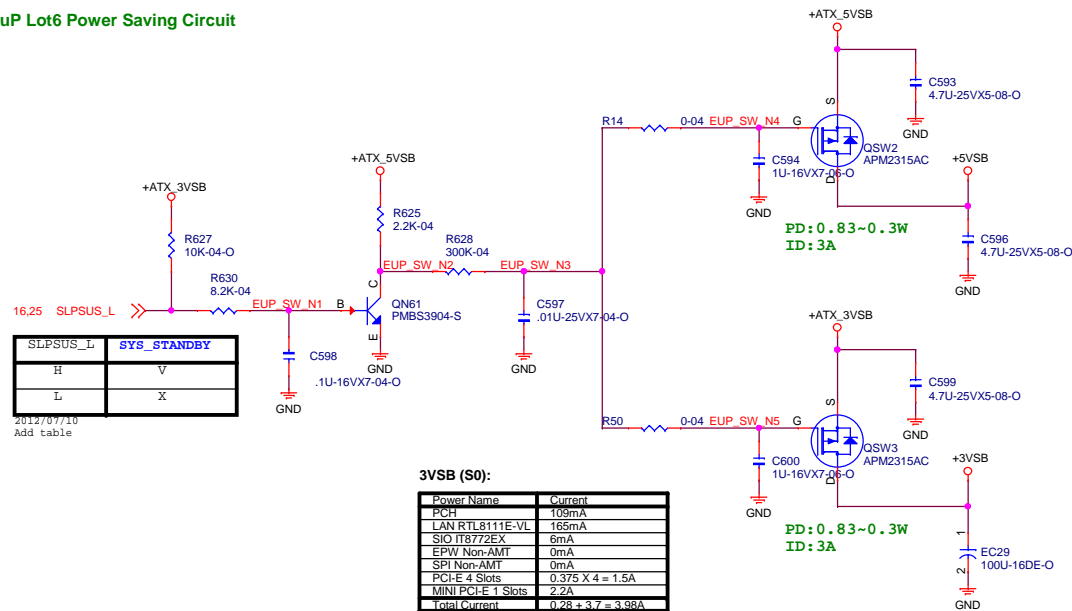


PCH ME power

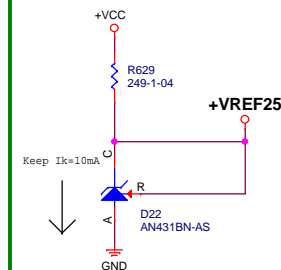
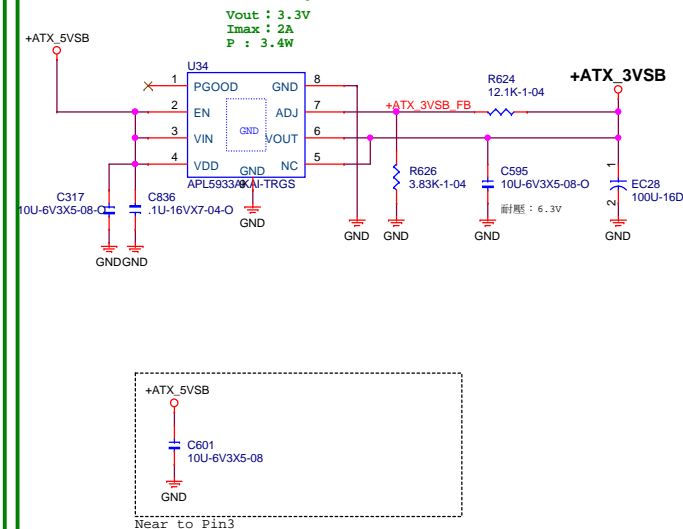
2013/1/10 Wilson: Del ME POWER circuit



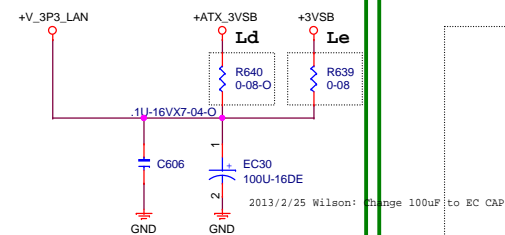
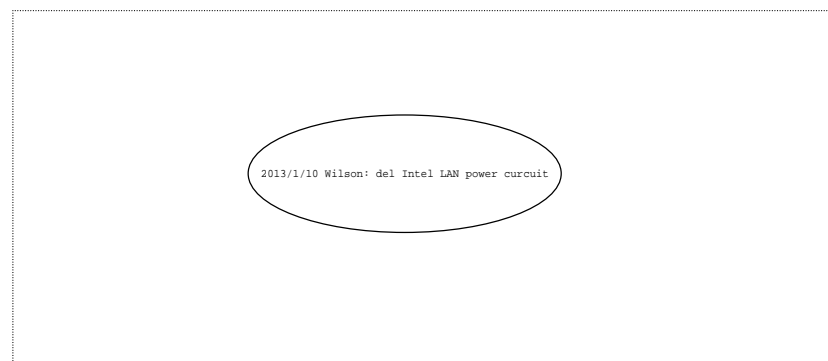
EuP Lot6 Power Saving Circuit



+3V Standby



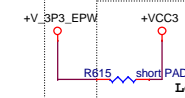
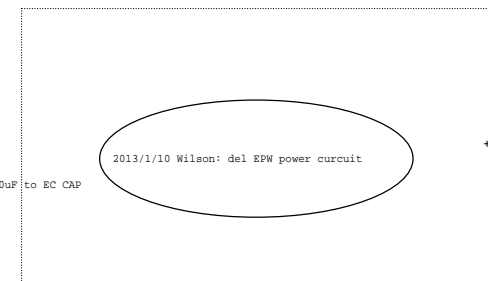
LAN Power Circuit



LAN Power Source

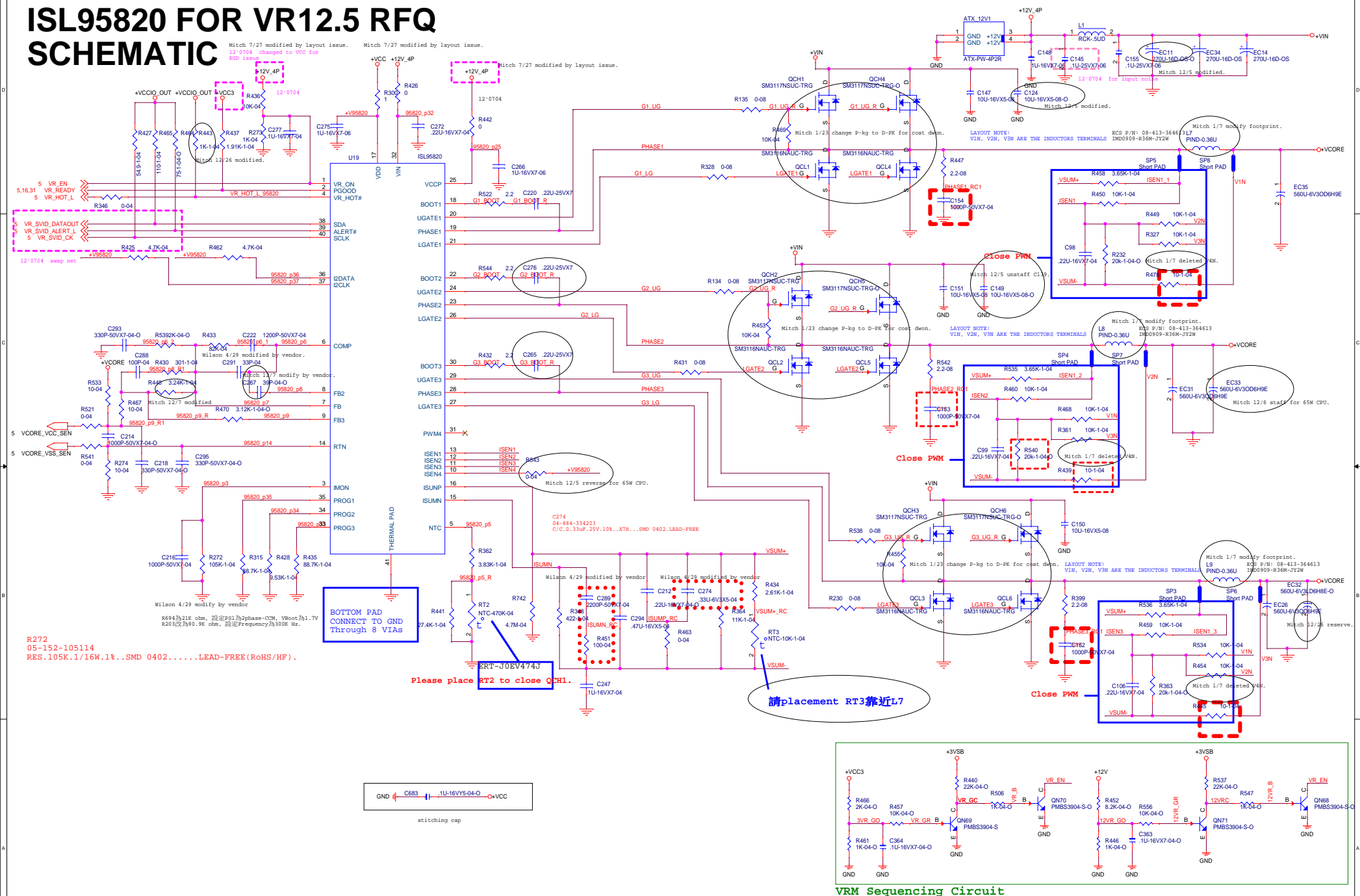
	EUP Enable G3-->X5_25	La	Lb	Lc	Ld	Le
Intel LAN	can wake up	V	V	X		
	can't wake up	V	X	V		
Realtek LAN	can wake up				V	X
	can't wake up				X	V

SPI ROM & PCH Power Circuit



+VCC3_EPW	Ld	Le	Lf
Intel LAN	X	V	X
Realtek LAN	V	X	X
Intel LAN(Cost down)	X	X	V

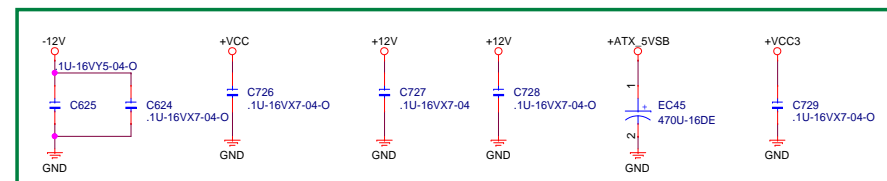
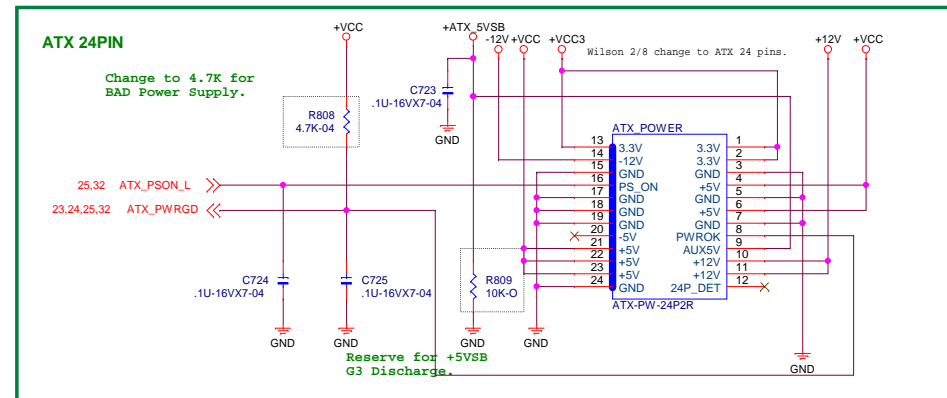
ISL95820 FOR VR12.5 RFQ SCHEMATIC



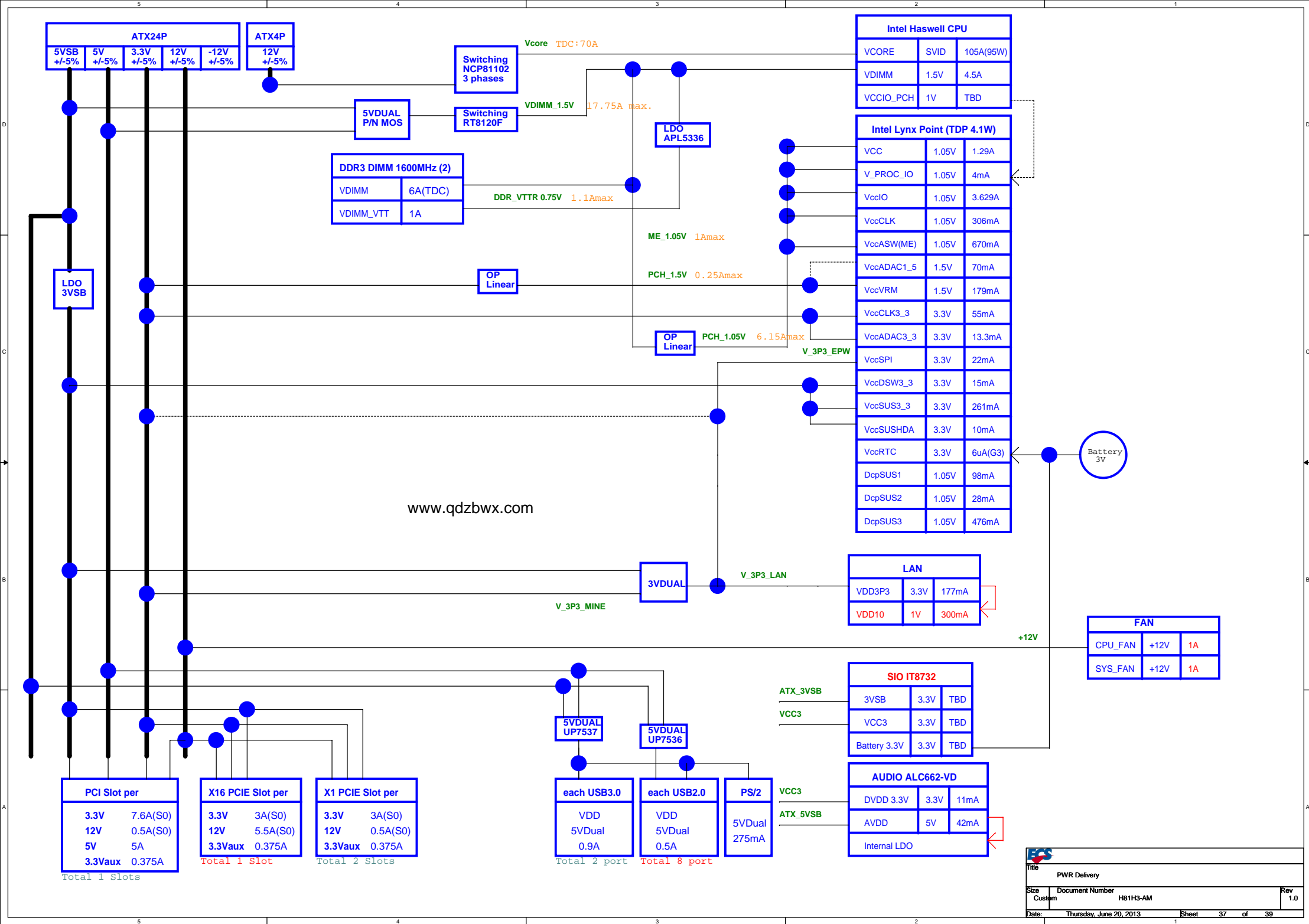
VRM Sequencing Circuit

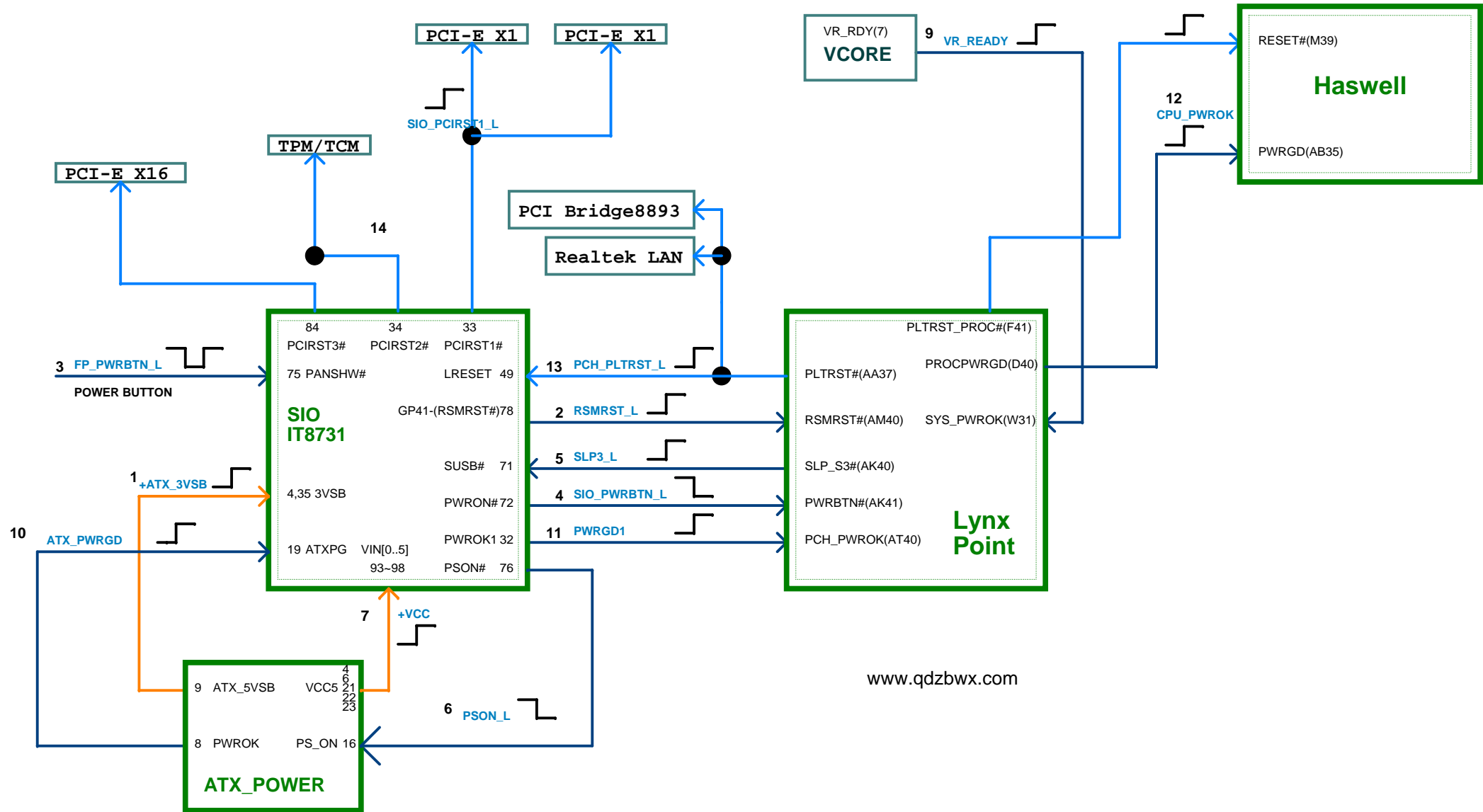
Title			
VR12.5 SOLUTION ISL95818 SUGGEST SCHEMATIC			
Size C	Document Number H81H3-AM	Rev 1.0	
Date:	Friday, June 21, 2013	Sheet	35 of 39

Wilson 2/8 Del VCC3 & VCC DC/DC switching



07/18 Change to 12P-Anthony





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